Non-random device mismatch considerations in nanoscale SRAM

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***Abstract*—Competitive density, performance, and functional objectives of the SRAM bit cell require design rules which are much more aggressive than those used in base logic designs. Because soft fail yield in SRAM is dependent on the device threshold and threshold mismatch in the bit cell, much research has been directed toward addressing the random contributors to within-cell device threshold variation. We examine four sources of potential non-random threshold mismatch that can arise from the use of aggressive design rules in the bit cell; (1) implanted ion straggle in SiO2, (2) polysilicon inter-diffusion driven counter-doping, (3) lateral ion straggle from the photo-resist and (4) photo-resist implant shadowing. Using simulation and hardware measurements, we quantify the device parametric impacts and provide a statistical treatment forming the basis for quantification of the functional margin impacts on the bit cell. We examine two lithography compliant bit cell layout topologies and quantify the impact of systematic mismatch on the margin limited yield.**

***Index Terms*—SRAM, SNM, Write Margin, statistics, bit cell, technology scaling, variation.**

I. Introduction

The 6T SRAM bit cell has become an integral part of each technology offering and a benchmark of technology competitiveness in today's VLSI microelectronics industry. A significant source of variation in nanoscale CMOS technologies is associated with random dopant fluctuations (RDF), which follows a $1/\sqrt{WL}$ relationship. Although high-k/metal gate technologies have provided some relief, aggressive design rule and device scaling has led to an increase in device variation in both SRAM and logic devices. Because it is common for the SRAM devices to be near or below minimum logic design rules, the RDF mismatch phenomenon is exacerbated. Additionally, pushed design spacing rules used in the dense SRAM cell can lead to added sources of variation that is not observed in circuits designed with the standard logic design rules.

Although the SRAM devices and logic devices are built concurrently using the same processing steps, often sufficient differences exist so that separate BSIM device models are required for the SRAM devices. This may be attributed to several factors. First, there may be intended deltas due to the use of additional Vt tailor steps to fine tune the SRAM threshold voltage for optimal functional (yield) margin, performance, or leakage optimization reasons. The second reason is non-intentional and is attributed to the process, structural differences, STI stress, and a range of proximity effects. For these reasons, commercial nanoscale CMOS technology suppliers provide a set of unique models for the SRAM cell devices that accompany the supplied bit cell. These additional sources of variation may also contribute to non-random or systematic mismatch within the SRAM cell.

As scaling continues beyond the 32nm node, the pushed rules used in bit cell design will warrant increased attention and more costly measures to avoid sources of systematic, non-random device mismatch. We define non-random mismatch as a mean offset in the device pair (e.g. pull down NMOS Vt left vs right) within the same or adjacent bit cell. Factors which may contribute to non-random mismatch are layout topology, process scaling practices, and use of pushed design rules in the bit cell.

In this paper we consider the implications of cell layout topology, process scaling, and pushed design rules on device variation in present and future nanoscale SRAM. Four specific alignment sensitive mechanisms which may impact non-random device threshold mismatch are evaluated. Experimental data and process simulations are used to both highlight and quantify sources of non-random mismatch. A statistical basis is provided as a foundation for quantifying the functional margin impacts of non-random device variation on the bit yield. Based on an examination of existing 6T layout options, and consideration of non-random mismatch sources, we examine the relative merits of an alternative layout, possessing different symmetry, and area limiting design rules from the topology used in today's dominant industry layout.

II. 6T Cell topologies

The optimal 6T layout topology will be dependent on many factors. These include processing capability, performance, density, power, and functional requirements. There are, at least initially, a number of options theoretically available for placing 6 transistors to perform the desired function. A summary provided by Ishida is reproduced in Fig. 1 for this discussion [1]. Following the nomenclature of Ishida, although published examples of type 2 and 3

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can be found, the cell type 1a was the dominant industry topology across several nodes prior to 90nm. At technology nodes below 90nm, the type 4 cell topology became (and remains) the dominant industry cell design.

A. Lithographic considerations

As scaling continues below 90nm, the lithographic challenges in printing and controlling the dimensions within the same printed layer in orthogonal directions has become increasingly difficult [2]. This has led to restrictions in layout orientation and shape for printed layers requiring tight dimensional control. For the SRAM devices it is therefore advantageous for the active single crystal regions and gate layer to be printed orthogonally, thus allowing optimal dimensional control for these layers. Of the cell topologies or types summarized by Ishida, only type 4 and a variation on type 1-b provide this advantage. For this reason we will explore both design topologies in more detail. Fig. 2 compares the dominant industry layout (type 4) with an alternate style (1x), Fig. 2(b), that also complies with the layout restrictions in sub 90nm designs.

Table-1: Variations of the inverter layouts and SRAM cell layouts.

	Category 1	Category 2	Category 3	Category 4
Layouts of Inverters				
Layouts of SRAM Cells	Type-1a cell Type-1b cell	Type-2 cell	Type-3 cell	Type-4 cell

Description of Symbols: Vss, Vdd, Strage Node, Gate Electrode

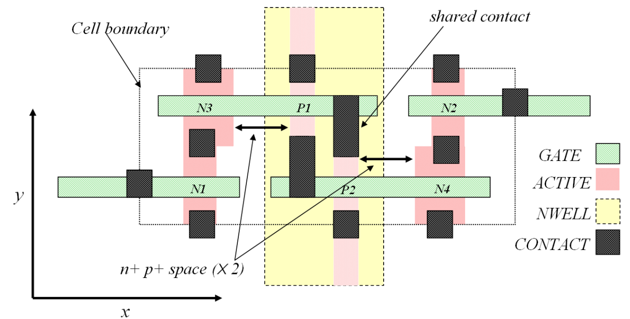
Fig. 1. Summary of 6T cell layout topologies (©IEEE '98) [1].

B. Bit cell dimensions

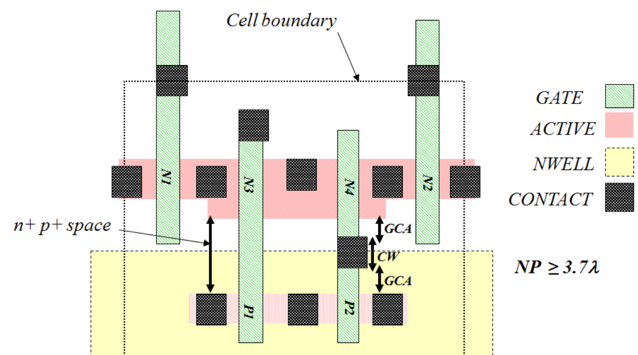
Because of the design symmetry for both type 4 and 1x topologies, the bit cell area can be expressed as the product of the cell boundary dimensions $Xcell$ and $Ycell$.

$$Acell = Xcell \cdot Ycell \tag{1}$$

A list of the limiting pushed design rules representative of those used in advanced silicon dense SRAM cells is given in Table I [3][4]. Although some deviation will be expected as technologies evolve, the rules are expressed



(a) Dominant industry bit cell design (topology 4).



(b) Alternate bit cell design (topology 1x).

Fig. 2. Example layouts of 6T SRAM bit cell topologies 4 (a) and 1x (b). Alignment of NWELL layer and subsequent block level layers will be asymmetrical with respect to devices N1, N3 and P1 compared with devices N2, N4 and P2 for topology 4. The n+ to p+ space for the 1x topology is limited by rules GCA and CW as shown in (b).

as function of the technology node (λ) to capture the effect of scaling. Although these pushed rules are consistent with those used in industry, some differences will exist between technology suppliers to allow optimization of yield and parametric values as desired. We use (Wpd/Lpd),(Wpg/Lpg),(Wpu/Lpu) to refer to the width and length of the pull down NMOS, pass gate NMOS, and pull up PMOS devices respectively. Consistent with (1), the type 4 bit cell area is the product of (X_4) and (Y_4). The dimension (X_4) for design topology 4, illustrated in Fig. 2(a), becomes:

$$X_4 = 2 \cdot (\frac{1}{2}(TT) + (GPA) + max(Wpd, Wpg) + (NP) + Wpu + \frac{1}{2}(AA)) \tag{2}$$

and the dimension (Y_4) is:

$$Y_4 = (2(CW) + 4(GC) + max(Lpd, Lpu) + Lpg) \tag{3}$$

Following the substitutions provided in Table I, the bit cell area for topology 4 is expressed as a function of device dimensions and technology node dimension:

$$A_4 = (8.3\lambda + 2 \cdot max(Wpd, Wpg) + 2Wpu) \cdot (5.6\lambda + max(Lpd, Lpu) + Lpg) \tag{4}$$

An alternative (1x) topology, which also conforms to the lithographic constraints previously discussed is shown in Fig. 2(b). Following the limiting design rule analysis as before:

$$X_{1x} = 2 \cdot (2(CW) + 4(GC) + Lpg + Lpd) \tag{5}$$

$$\begin{aligned} Y_{1x} = GPA + \frac{1}{2}(TT) + max(3.75(M1P), \\ (GCA) + \frac{3}{4}(M1P) + Wpd + (NP) + Wpu) \end{aligned} \tag{6}$$

and by substitution, Table I, simplifies to:

$$\begin{aligned} A_{1x} = (11.2\lambda + 2Lpg + 2Lpd) \\ \cdot(1.5\lambda + max(10.5\lambda, Wpd + (NP) + Wpu)) \end{aligned} \tag{7}$$

Scaled device dimensions are approximated in Table II to enable a numerical area estimate. Although the scaled device dimensions will vary, depending on the specific fabricator device characteristics and bit cell performance and leakage targets, the measured differences in device dimensions make up a relatively small component of the overall bit cell area. We define the device packing factor (DPF) as the total channel area of the six transistors divided by the cell area to give a measure of the efficiency of the bit cell design for a given set of device dimensions. A larger DPF implies a more area efficient cell design. For today's competitive 6T dense SRAM the DPF is on the order of 9%. The DPF for the type 1x (assuming common device dimensions) is 6%.

A graphical summary of published bit cell areas from 90nm to 22nm is provided in Fig. 3. The calculated area for type 1x (equation (7)) is approximately 50% larger than the type 4 (equation (4)). This is due, at least in part, to two reasons, 1) the design rules used in this analysis (consistent with those in use today) are optimized for type 4, 2) the shared contact feature, allowing a very effecient cross couple interconnection in type 4. The Y_{1x} dimension is limited by the metal 1 and contact rules, resulting in a larger $Ycell$ dimension than otherwise required given the device widths and n+ to p+ spacing given in Tables I and II. Also, these rules have evolved and been optimized for the topology 4 design and will therefore tend to skew a direct comparison of area in favor of this common industry topology. If the design rules were more tailored for the 1x topology, this gap in area may be reduced.

The predicted cell area based on the pushed design rule and device scaling factors given in Table I and II show a good fit down to 32nm for the type 4 cell topology. Although only one published value is found for 22nm [5], the area of this type 4 cell design is becoming closer to the area expectation for the type 1x design. As we discuss later, the 1x topology offers some advantages over the type 4 for process complexity and susceptibility to the sources of non-random mismatch associated with the more aggressive n+ to p+ space. Based on the scaled rules given in Table I and II, the type 4 topology offers improved density and a shorter (lower capacitance) BL. The bit lines extend in the y-direction for type 4 and in the x-direction for type 1x.

TABLE I
SRAM BIT CELL DESIGN RULE SCALING ASSUMPTIONS

Design rule	symbol	Dimension (λ)
Gate to contact space	(GC)	0.7
Gate past active	(GPA)	1
Gate tip to tip	(TT)	1
Gate contact to active	(GCA)	1
Contact size	(CW)	1.4
p+ to p+ space	(AA)	1.7
n+ to p+ space	(NP)	1.8
M1 pitch	(M1P)	2.8

TABLE II
SRAM BIT CELL DEVICE DIMENSION SCALING ASSUMPTIONS

Cell device	symbol	Dimension (λ)
Pull down NMOS width	Wpd	2.5
Pull down NMOS Length	Lpd	0.9
Pull up PMOS width	Wpu	1.4
Pull up PMOS Length	Lpu	0.9
Pass gate NMOS width	Wpg	1.7
Pass gate NMOS	Lpg	1.1

C. Process features

The shared contact feature, commonly used in topology 4 [6] [4] [7] [8], facilitates a higher DPF compared to 1x, and significantly improves the area efficiency of the cross coupled connection . While providing an advantage in area and DPF, the shared contact feature does add a degree of processing and lithography complexity above that of a logic-only process. Because this feature is typically only allowed in the well-controlled dense SRAM environment, a degree of commonality with pure logic processing is lost with topology 4 while the topology 1x is compatible with a logic-only process and does not require this process feature.

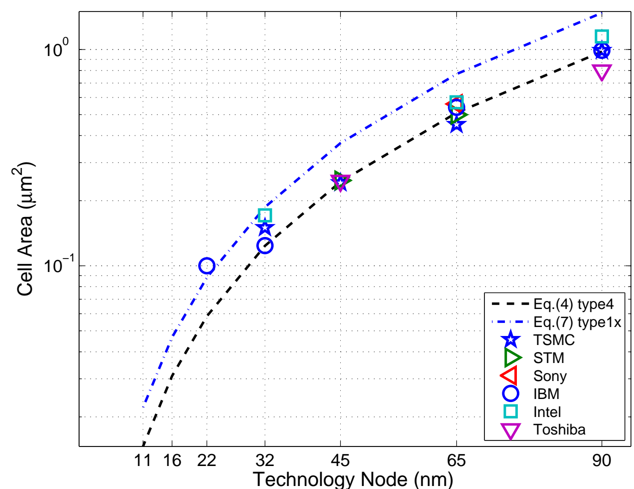


Fig. 3. Dashed lines show SRAM bit cell areas by technology node for topology 4 and 1x based on scaled design rules and device dimensions given in Tables I and II. Published 6T cell areas by technology node are beginning to deviate from the values predicted by (4) at 32 and 22nm.

In addition to the shared contact process feature, differences may also arise from the fact that the device pairs reside in separate active silicon islands for the topology 4 design. Although there are several potential consequences of this difference, a unique behavior in radiation induced soft error response has been observed when the separate silicon islands also share separate wells [9]. In contrast, the active silicon islands are shared for the device pairs for the 1x topology.

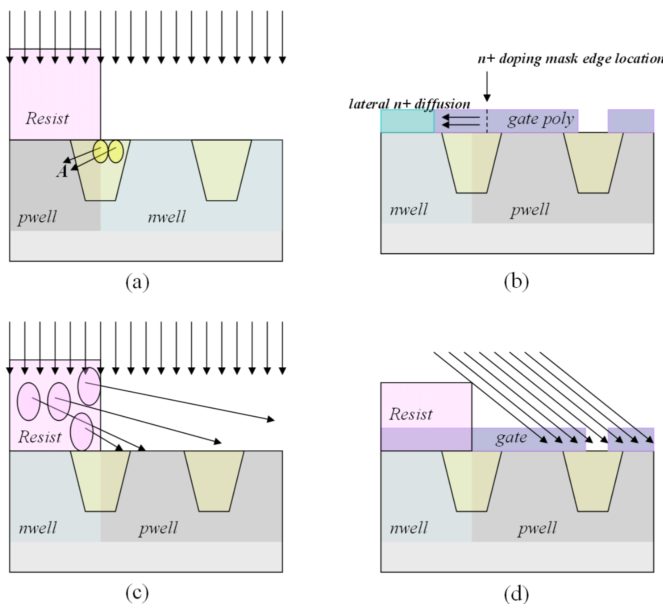


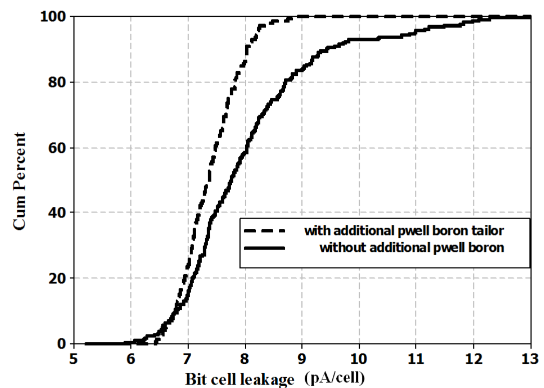
Fig. 4. Schematic depiction of four alignment sensitive sources of potential non-random mismatch in SRAM devices. (a) Lateral straggle within SiO_2, (b) lateral counter-doping in gate polysilicon, (c) lateral straggle from resist sidewall, (d) halo shadowing.

III. Scaling and sources of alignment sensitive mismatch in dense SRAM

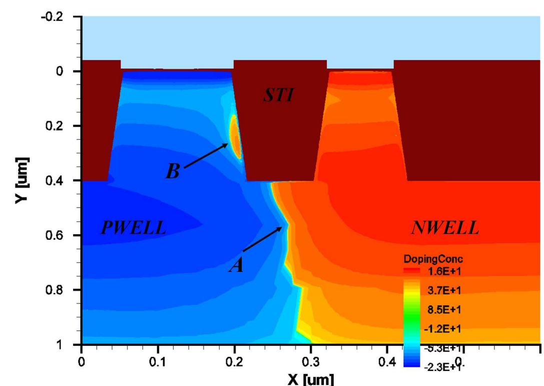
Because of its advantage in density, the type 4 topology remains the dominant cell design in the industry and has been successfully migrated across technology nodes (90nm to 32/28nm) in both bulk and SOI. However, a careful investigation of the ramifications of the continued scaling of this cell topology is warranted. In addition to added processing complexity associated with the shared contact for this cell topology, the n+ to p+ space is a cell area-limiting rule and appears twice in the cell (x) dimension, Fig. 2(a). As a result, the design rules associated with this space are aggressively pushed. We will now discuss how this can lead to a higher sensitivity to sources of non-random or systematic mismatch.

As scaling continues below 32nm reduced dimensions required for the SRAM bit cell using pushed rules will place increased demands on the alignment and printed dimension tolerances required for large scale SRAM arrays. This is because of the yield sensitivity to the mismatch in device threshold, and any systematic mean shift or variance which is non-random ($\mu_{Vtmm} \neq 0$) will impact the soft fail limited yield.

Because of fundamental symmetry differences in the topology 4 and 1x,as shown in Fig. 2, the mismatch characteristics can be different. This is due to the relationship between the block level resist boundary location (indicated by the drawn NWELL layer) and the devices within the cell. For example, the PD NMOS devices in the type 4 cell are located on opposite sides of the well. Any shift in the alignment of the well resist (NWELL or PWELL), gate pre-doping mask, halo masks or source/drain implant block mask can result in a within cell PD device mismatch. This is because all of these masks share a similar pattern and orientation. Following this example, using the PD device again to illustrate, in the 1x cell the PD NMOS devices are on the same side of the well boundary. A shift in the alignment of the resist masks will tend to produce a symmetrical within-cell shift resulting in a zero net within cell mismatch.



(a) Measured cell leakage distribution (plotted as percent cumulative distribution on the y-axis) based on 24k array showing increased leakage due to lateral straggle of phosphorus in SiO_2 during NWELL implant.



(b) Simulated PWELL counter-doping due to lateral straggle of phosphorus in SiO_2 during NWELL implant with 30nm mask misalignment.

Fig. 5. (a)Measured electrical impact on 65nm SRAM 24K array leakage due to lateral straggle of NWELL phosphorus in the STI. (b) Simulated well contours showing effects of transverse straggle in SiO_2 on the adjacent PWELL with 30nm misalignment of the NWELL resist using 45nm pushed rules. Area labeled A is normal PWELL/NWELL boundary, area B is counter-doped (n-type) region in PWELL resulting from phosphorus lateral implant straggle in STI.

The potential for alignment related mismatch sources is an important consideration in future bit cell design. This can arise from several factors, and the type 4 topology, while possessing a significant DPF advantage over the alternatives, is particularly vulnerable to this issue for reasons previously discussed. Fig. 4 illustrates four alignment driven sources that can introduce non-random sources of mismatch, (a) transverse or lateral straggle in SiO_2 [10], (b) polysilicon inter-diffusion driven counter-doping [11] [12], (c) lateral ion straggle from the photo-resist [13] [14] [15], and (d) photo-resist implant shadowing [16] [17]. Of these four mechanisms, (a) and (c) originate from higher energy well formation implant conditions used in bulk CMOS processes while (b) and (d) are consistent with both bulk and SOI process technologies. In the following sections we investigate these mechanisms and their impact on the SRAM devices. Hardware data and process simulations are used to quantify the extent of mismatch from each of the mechanisms.

A. Lateral straggle in SiO_2

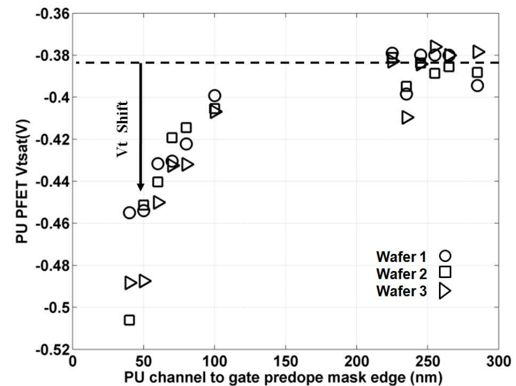
The potential impact of transverse straggle in the SRAM cell devices arises from the aggressive n+/p+ space used in the cell to gain density. Lateral ion scattering in the shallow trench isolation (STI) oxide from the higher energy well implants can counter dope the adjacent well edge (e.g. point A in Fig. 4a). The PD NMOS and PU PMOS devices are most likely to be impacted due to their proximity to the well edge. Fig. 5(a) shows the measured impact on the average bit cell leakage, as measured in a 24k-bit array. Although several methods of avoiding this mechanism can be taken, introducing an additional boron implant into the PWELL at the appropriate depth, $\approx$ 100nm in this case, can be used to mitigate the electrical impacts.

Using dimensions and implant profiles consistent with 45nm designs (n+ to p+ space of 90nm) an NWELL mask misalignment of 30nm is sufficient to create a substantial counter-doping path between the source and drain of the adjacent PD NMOS device, Fig. 5(b). As scaling continues beyond 45nm, the well profiles in bulk technologies will require optimization along with aggressive well alignment and image size tolerances to prevent this mechanism from impacting future SRAM devices.

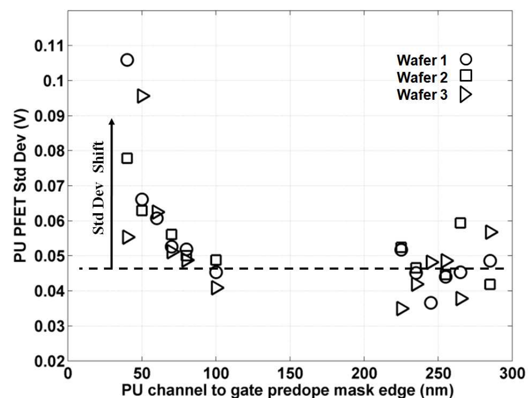
This mechanism will impact devices only on one side of the cell for the type 4 topology, thus creating a non-random device mismatch within the cell. Because the n+ to p+ space is not a limiting rule for the type 1x cell, this mechanism is much less likely to be a concern. Due to the symmetry properties of the type 1x cell, if lateral ion straggle in the STI were to penetrate into the opposite polarity well, non-random mismatch would be observed between devices in adjacent bit cells.

B. Polysilicon inter-diffusion

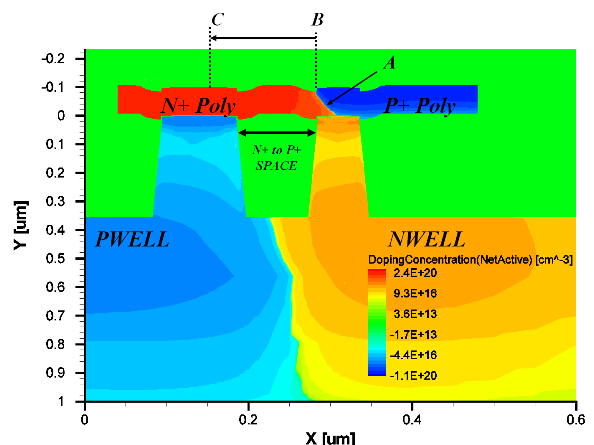
Although migration to metal gate began to occur at the 45nm node, some fabricators have opted to remain with polysilicon gate electrodes [18]. Polysilicon inter-diffusion



(a) Measured PU PMOS $Vtsat$ vs gate predoping mask proximity(distance B to C in Fig. 6(c). PMOS $|Vt|$ increases as the poly predoping mask edge (C) becomes closer to the PMOS channel edge (B).



(b) Measured PU PMOS $Vtsat$ standard deviation vs gate predoping mask proximity (distance B to C in Fig. 6(c). A pronounced increase in Vt variation is observed as the gate predoping mask edge (C) becomes closer to the PMOS channel edge (B).



(c) TCAD simulation showing phosphorus encroachment over pull up PMOS channel in 45nm SRAM.

Fig. 6. Effect of proximity to gate predoping mask edge on (a) PU PMOS Vtsat (b) PU PMOS Vt standard deviation. Measured data from 65nm process technology. (c) Cross section simulation illustrating the concern with poly inter-diffusion across the narrow n+/p+ space in the dense SRAM environment with type 4 cell topology. Region A shows the phosphorus encroachment over the channel region of the pull up PMOS device altering the PMOS gate work function and threshold voltage (μ, σ).

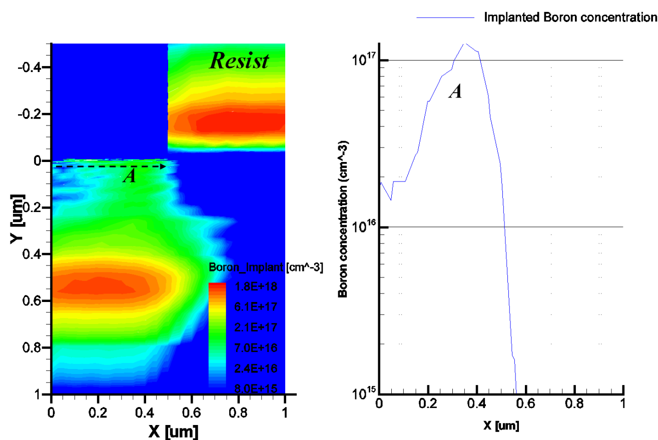


Fig. 7. Doping contour plot following an atomistic Monte Carlo simulation of the PWELL deep implant (left). Variation in boron concentration across the silicon surface as a function of proximity to resist edge (right). Doping profile taken at a depth of approximately 50nm. The resist is located from 0.5μ to 1μ on the X axis. Boron lateral straggle emanating from the resist sidewall region during deep PWELL implant results in near-surface concentration variation across the PD NMOS channel region (A).

is also significant concern with scaling as n+/p+ space is aggressively pushed. The practice of using a poly pre-doping step is commonly used to insure the n+ polysilicon is degenerately doped. The alignment of this pre-doping mask as well as the n+ and p+ source drain implant masks must be carefully placed to avoid diffusion induced counter-doping of the gate above the channel region of the complementary device as shown in Fig. 6(c). Because the diffusivity is significantly higher along the grain boundaries in the polysilicon than in the single crystal, and because of the proximity of physical layout, gate counter-doping can occur. Scaling the lateral dimensions without reducing the thermal budget or alignment tolerance and/or bias will increase the sensitivity to the mechanism with scaling. Fig. 6(a) shows the shift in PMOS Vt_{sat} as a function of proximity to the gate predoping mask. Because the gate workfunction is also impacted, the standard deviation of the PMOS Vt_{sat} increases with phosphorus encroachment in the gate over the PMOS channel region, Fig. 6(b). The data from three individual wafers, shown in Fig. 6(a) and 6(b) reflects the wafer-to-wafer variation observed. The three wafers were processed together in the same lot and had the same nominal process conditions.

For the type 4 layout topology, this mechanism can result in an asymmetric mean shift in the pull up PMOS Vt as well as an increase in the variance of the Vt due to the impact on the work function component of the variance in the threshold voltage as described in (14). Because of the inherent sensitivity of this mechanism to the n+ to p+ space, the 1x topology would provide relief in allowing a more relaxed alignment and image tolerance specification.

C. *Lateral ion straggle from the photo-resist*

The physical mechanism of lateral dopant straggle stemming from nuclear collisions of the high energy implant species in the photo-resist has been previously documented [13]. Depending on the implantation species and acceleration energy, this mechanism can impact devices in proximity to the well edge at distances exceeding 1μm. Because of this, this mechanism can impact both logic devices as well as the devices in the dense SRAM cell. For bulk technologies requiring higher dose and energy well implants the effect is more significant.

The amount of near surface doping is proportional to the dose of the high energy implant used in the formation of retrograde wells. As shown in Fig. 7, using implanted B11 energy of 200keV with a dose of 3E13 at/cm^2, the near-surface doping is a function of the distance from the resist sidewall.

Because the surface concentration is a function of the distance from the resist sidewall, there is an alignment sensitivity for the SRAM devices. Because of the higher channel doping levels and use of thin oxide devices used in most nanoscale SRAM cells, provided deep retrograde implant doses are kept in this range, the impact of this mechanism on nanoscale CMOS SRAM is expected to be limited.

Because of the longer range nature of this mechanism, the 1x and type 4 topologies will be impacted to a similar degree. The implications of this proximity mechanism for the bit cell are two fold. First, this mechanism can introduce a threshold voltage offset in the SRAM devices with respect to isolated logic devices and second, it is an additional source of non-random mismatch and variation in channel doping.

D. *Photo-resist implant shadowing*

Because of the photo-resist thicknesses during the halo implant step, implant shadowing is another physical mechanism that becomes nearly unavoidable in the dense SRAM designs. The halo or pocket implant, used to control short channel effects, is commonly implanted at angles in the range of 30-45 degrees as a quad implant. Because of the pushed rules in the SRAM cell, the thickness and proximity of the photo-resist will result in some degree of implant shadowing in the dense SRAM devices. This has the potential of inducing threshold voltage shifts in the SRAM devices relative to the logic devices and for the type 4 topology, can also become a source of non-random mismatch. In addition to alignment, this mechanism has the added variation components of resist thickness, and surface corner rounding.

With the resist thicknesses and design rules used in high density SRAM, halo shadowing, Fig. 4(d) will occur for at least one of the 4 quad implants for the PD and PG NMOS devices. This shadowing effect is illustrated in the drawing shown in Fig. 8. The fraction of the PD NMOS device width (f_{shadow}) that is shadowed is given by:

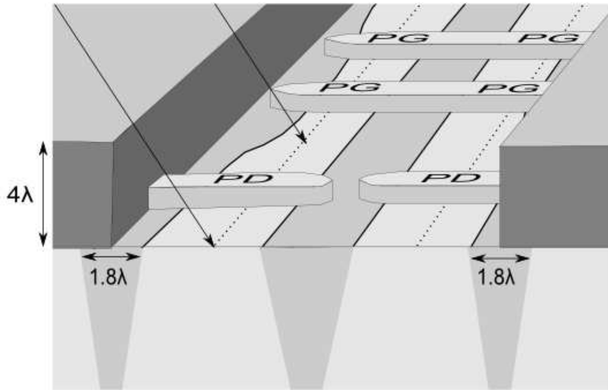


Fig. 8. Illustration showing effect of halo mask shadowing on array segment of SRAM NMOS devices. (Mask edge is orthogonal to gate consistent with the cell design shown in Fig.2(a).)

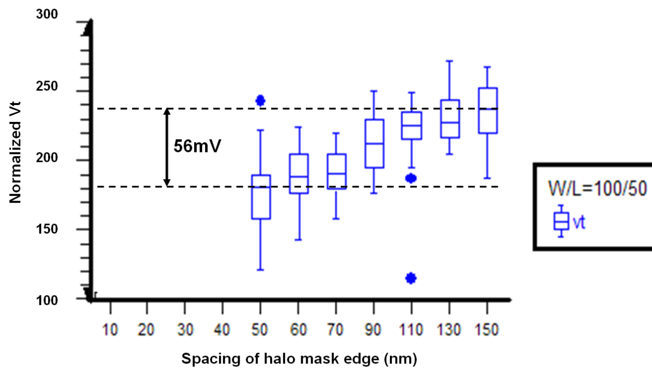


Fig. 9. Measured hardware data showing effect of halo mask shadowing on narrow NMOS threshold voltage from 65nm process technology. (Mask edge is orthogonal to gate consistent with Fig.2 and with the 3-D drawing shown in Fig. 8.)

$$f_{shadow} = \frac{(H_r) \cdot tan\theta - (NP)/2}{Wpd} \quad (8)$$

where H_r is the resist thickness, θ is the halo angle. For a typical halo resist thickness of (4λ) with a 30 halo angle, and using (NP) and Wpd values provided in tables I and II yields a f_{shadow} value of 0.56. This means that more than half of the PD NMOS device is being shadowed under nominal process conditions. Any misalignment will result in a mismatch in the fraction of the device shadowed which will in turn translate into within cell mismatch for the type 4 cell topology.

TCAD simulations of a narrow 45nm NMOS indicate that this effect can be on the order of 50mV for a fully shadowed halo in the direction parallel with the polysilicon. Measured electrical results Fig. 9 are approximately consistent with the process simulation results and show a 56mV delta threshold voltage when the single quad halo (parallel with the gate) is fully blocked.

Due to the symmetry of the type 4 cell, halo block mask misalignment will result in a within-cell device threshold imbalance. As with the other alignment sensitive mechanisms previously discussed, use of a more aggressive n+ to p+ space will need to be compensated with improved alignment and/or image tolerance improvement to reduce the sensitivity to mismatch associated with this mechanism.

E. Mechanism impact summary

Table III summarizes the process dependencies, SRAM devices impacted, and compares the net effect differentiated by cell topology choice for each of the four mechanisms investigated. The net device impacts associated with the four mechanisms previously discussed will be dependent on the bit cell symmetry. Due to the symmetry differences between topology 4 and 1x, any deviation in alignment will translate directly to either a mean shift between device pairs within the cell or adjacent cell to cell device mismatch. The net measured effect of non-random mismatch is identified by the observation that $(\mu_{Vtmm} \neq 0)$ for the local device pairs.

In addition to non-random mismatch, the standard deviation in Vt is also impacted by these mechanisms. The increase in standard deviation, as observed with polysilicon gate interdiffusion, can be large, Fig. 6(b), if the image tolerance, alignment, and additional processing dependencies such as temperature, grain boundary diffusion, and implant dose are not well controlled.

While all four systematic mismatch mechanisms identified are dependent on the n+ to p+ space, because type 1x cell area is limited by rules other than n+ to p+ space, the impact (assuming similar alignment and image tolerances) will be eliminated or significantly reduced for the 1x design relative to type 4. The amount of reduction will depend on the fabrication process details, in-line controls, the specific mechanism, and degree to which the n+ to p+ space can be optimally relaxed.

The density advantage of the type 4 topology would permit, if desired, optimized trade off of either increasing the n+ to p+ space or tightening the alignment and image tolerances of the implant blocking resist levels involved. Although the n+ to p+ space only occurs once in the Y_{1x} dimension, the 1x topology does not offer an intrinsic advantage in sensitivity to the n+ to p+ space. Taking the derivative of area with respect to (NP) for both topologies, equations (2) - (6), reveals that $2 \cdot Y_4$ is equal to X_{1x} when $(Lpu = Lpd)$. Once the n+ to p+ space becomes a limiting rule, both topologies are equally impacted. Because of the rules used for contacted gate to active area, the n+ to p+ space is much more relaxed in the 1x topology.

IV. Non-random variation: Statistical infrastructure

A statistical infrastructure to establish the relationship between mismatch and margin limited yield is outlined in this section. To assess the impact of the non-random mismatch, we will treat the device threshold (Vt) as a continuous random variable. The 6T SRAM margin

TABLE III
DEPENDENCIES AND IMPACTS OF FOUR MECHANISMS OF NON-RANDOM MISMATCH

MECHANISM	PRIMARY DEPENDENCIES[a]	DEVICES IMPACTED	TOPOLOGY 4 **within cell** mismatch	TOPOLOGY 1x **adjacent cell** mismatch
Implant straggle in SiO_2	Well dose, energy, species	PD,PU	$\mu_{Vtmm} \neq 0, \sigma_{Vt,DF} \uparrow$	$\mu_{Vtmm} \neq 0, \sigma_{Vt,DF} \uparrow$
Polysilicon inter-diffusion	Temp, dose, diffusivity	PU	$\mu_{Vtmm} \neq 0, \sigma_{Vt,GWF} \uparrow$	$\mu_{Vtmm} \neq 0, \sigma_{Vt,GWF} \uparrow$
Lateral ion straggle in resist	Well dose, energy, species	PD,PG,PU	$\mu_{Vtmm} \neq 0, \sigma_{Vt,DF} \uparrow$	$\mu_{Vtmm} \neq 0, \sigma_{Vt,DF} \uparrow$
Halo shadowing	resist thickness, halo dose, angle	PD,PG,PU	$\mu_{Vtmm} \neq 0, \sigma_{Vt,DF} \uparrow$	$\mu_{Vtmm} \neq 0, \sigma_{Vt,DF} \uparrow$

[a]dependencies in addition to n+ to p+ space, alignment, and CD variation

variance (σ_M^2) can be expressed as the sum of the squared components comprised of each of the 6 transistors shown in Figure 2. For reasons covered in the previous section, the SRAM device pairs may not have identical variances and therefore should be treated independently for our analysis.

$$\sigma_M^2 = \sum_{i=1}^{6} \left(\frac{\partial M}{\partial Vt_i} \sigma_{Vti} \right)^2 \tag{9}$$

The margin value may refer to the read static noise margin (RSNM) or write margin (WM) for example. While it is commonly assumed that the population mean and variance of each of the 3 pairs of transistors in the cell are equal, we have shown that deviations from this assumption can occur and are influenced by cell topology, process scaling and the use of pushed design rules. The margin mean is expressed in terms of (Vt) using the truncated form of the Taylor series expansion [19] as:

$$\mu_M \approx M_{Vt_{nom}} + \frac{1}{2} \sum_{i=1}^{6} \frac{\partial^2 M}{\partial Vt_i^2} \sigma_{Vti}^2 \tag{10}$$

The margin ($M_{Vt_{nom}}$) value at nominal Vt, refers to any margin which has a primary dependency on the device threshold. The margin limited yield may then be assessed by determining the fail probabilities. By accounting for the mean and variance components individually the fail probability is computed from the standard normal probability distribution function (PDF). When no systematic or non-random Vt mismatch exists, the probability of failure (P_T) for the bit cell is expressed as:

$$P_T[M \leq 0] = 1 - \int_0^{\infty} f_x(x)dx \approx erfc \left(\frac{\eta_{\sigma_M}}{\sqrt{2}} \right) \tag{11}$$

where η_{σ_M} is defined as $(\bar{M} - 0)/\sigma_M$. The probability is computed assuming a symmetrical 2-tail distribution to account for both states of the bit cell. When non-random Vt asymmetry exists, the fail probability for the left (P_L) and right (P_R) side of the cell must be considered independently. This is expressed as:

$$P_T[M \leq 0] = P_R[M \leq 0] + P_L[M \leq 0] \tag{12}$$

The yield for a large array with (N_b) bits is then computed from the binomial relationship. Assuming no redundancy, the yield is given as:

$$Y_M = (1 - P_T[M \leq 0])^N b \tag{13}$$

The margin mean and variance are explicitly dependent on the variance in device threshold voltage as described in (10) and (9). The more significant underlying components of the local variance in Vt are due to dopant fluctuations (DF), gate work function (GWF), and line edge roughness (LER). Treating these three components as independent random variables, the total variance is expressed as shown in (14).

$$\sigma_{Vt_{total}}^2 = \sigma_{Vt,DF}^2 + \sigma_{Vt,GWF}^2 + \sigma_{Vt,LER}^2 \tag{14}$$

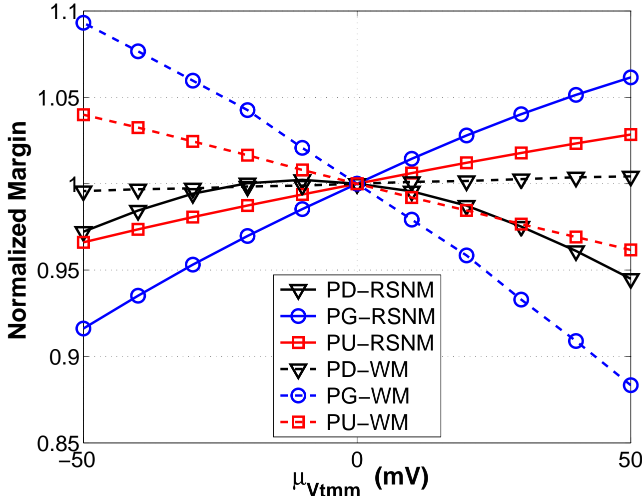
Processes or design topologies which are more susceptible to increases in the variance of any of these components are therefore less desirable. The dopant fluctuations (DF) are comprised of both random dopant fluctuations as well as any process induced systematic variations.

V. QUANTIFYING THE IMPACT OF NON-RANDOM MISMATCH ON YIELD

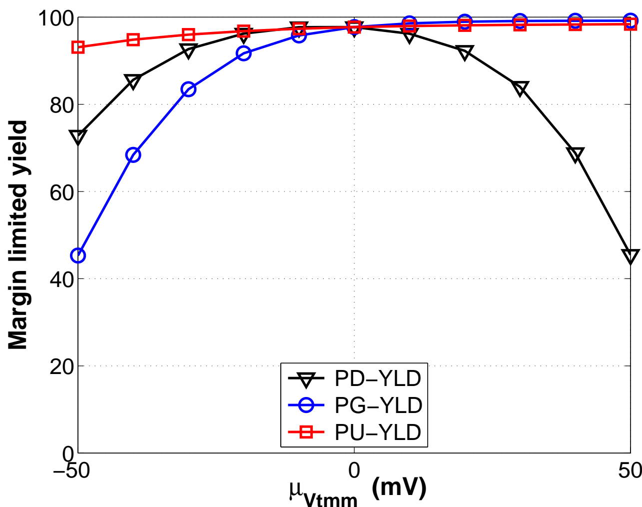
Random variation in device threshold is anticipated with an expected mean of zero for within cell mismatch. When non-random sources of mismatch produce a mean shift in $Vtmm$, such that ($\mu_{Vtmm} \neq 0$), an impact on the read static noise margin (RSNM) [20], or write margin (WM) may be observed [21]. To illustrate this, margin simulations are conducted using a commercial 45nm LP technology with the device dimensions given by Table II. The impact of μ_{Vtmm} on the mean RSNM and WM is plotted in Fig. 10(a). The margin limited yield, Fig. 10(b) for a 2 Megabit array is derived following (11), (12), and (13).

Given an equal amount of systematic mismatch, either within cell or adjacent cell-to-cell, a similar net yield impact is anticipated. This point is made by a consideration of the symmetries involved. For example, given the type 4 layout, the kinds of non-random mismatch described could result in the fail probability ($P[M \leq 0]$) for one of the two nodes becoming larger with respect to the other across the entire array. Alternately, for the type 1x symmetry, an adjacent cell-to-cell mismatch would be observed where the probability ($P[M \leq 0]$) for both nodes in every other cell in the array would be consistently increased. If both type 4 and 1x layout topologies were equally susceptible to the sources of non-random mismatch, the net impact on large array yield would therefore be negligible.

The effect of a non-random threshold shift (within cell or cell to cell), shown on the x-axis, is in addition to



(a) Impact of systematic mismatch on RSNM and WM (normalized).



(b) Impact of systematic mismatch on margin limited yield (2 Megabit).

Fig. 10. Impact of $\mu_{Vtmm} \neq 0$ on both RSNM and WM and margin limited yield. Simulations performed using on commercial 45nm LP technology SRAM models without the impact of increased variance.

the background random variation that is present in the statistical models. For this technology, the PG NMOS exhibited the highest degree of margin sensitivity. At nominal voltage (1.1V) and room temperature, this bit cell is RSNM limited therefore the yield degrades quickly as the PG NMOS Vt is lowered, Fig. 10(b). The RSNM and corresponding limited yield is adversely affected by both positive or negative shifts in the PD NMOS Vt. The PU PMOS has a more limited overall impact, lowering the RSNM limited yield as it becomes weaker.

VI. Identifying non-random variation

The detection of alignment driven non-random offsets may prove to be difficult following typical manufacturing test restrictions. Although a large sample size may be accumulated or exist for the bulk population, alignment will vary for individual lots. The sample size required to detect a 10mV offset in the sample mean ($\widehat{\mu_{Vtmm}}$) with 95% confidence will be on the order of 60 or more as given by (15) which may exceed the number of samples tested for a given lot or batch of wafers run with a given alignment. If we accept that alignment and printed dimensions are centered and normally distributed, the entire population of Vt mismatch (right - left) will also be Gaussian in distribution. Systematic offsets in image critical dimension (CD) or alignment will impact the total population.

The population standard deviation can be derived from the unbiased estimator, $\widehat{\sigma_{Vtmm}}$, having a confidence interval as defined in (16). A method using Fourier analysis to separate the global variation sources from short range (mismatch) sources such as random dopant fluctuations (RDF) can also be applied to the SRAM devices [22]. To quantify the base line Avt expectation for a given technology [23], care is taken to eliminate channel proximity to drawn corners, well edges or block-level-resist edges. Characterizing $\widehat{\sigma_{Vtmm}}$ for identically drawn device pairs in close proximity across a range a channel areas provides the technology base line for NMOS and PMOS devices.

SRAM device pairs within a cell or cell to adjacent-cell are in close proximity and are drawn identically, however they are subject to additional sources of variation. These additional sources of dispersion in mismatch may be attributed to the pushed rules and layout topology used in the 6T bit cell. For advanced nanoscale technologies the threshold mismatch values measured for larger L dimensions are observed to fall on a different slope than that of the minimum L [24] [25], therefore the Avt slope should be derived using the same L values as used in the cell.

Because the alignment sensitive occurrences of non-random mismatch can be limited to individual groups of samples, detection can be a challenge. A brief description of an approach for determining if such a condition exists is briefly summarized to illustrate a simple case where the sample variances can be assumed to be equal. Because the expected value of the paired data sample $(Vtr - Vtl)$ mismatch mean is always zero, this is the null hypothesis. The confidence interval for testing this hypothesis is given by:

$$\mu_{Vtmm} \pm t_{\alpha/2} \left(\frac{\widehat{\sigma_{Vtmm}}}{\sqrt{N}} \right) \tag{15}$$

where N refers to the sample size, $\widehat{\sigma_{Vtmm}}$ is the sample standard deviation and $t_{\alpha/2}$ is the test with specific significance, α with $(N-1)$ degrees of freedom. The χ^2 distribution may be used to determine the confidence interval on the sample variance. We express this confidence interval in the form of a probability as:

$$P\left[\frac{(N-1)\widehat{\sigma^2_{Vtmm}}}{\chi^2_{N-1,1-\alpha/2}} \leq \sigma^2_{Vtmm} \leq \frac{(N-1)\widehat{\sigma^2_{Vtmm}}}{\chi^2_{N-1,\alpha/2}} \right] = 1 - \alpha \tag{16}$$

where the probability P (with significance level α) that the population variance lies within the defined intervals is

defined by the χ^2 distribution.

VII. Conclusions

Dopant fluctuations in nanoscale SRAM devices may be attributed to both random and non-random components. Cell layout topology, process scaling, and pushed design rules used in dense SRAM bit cell designs can influence the susceptibility to non-random mismatch in present and future nanoscale SRAM devices. We investigated four potential sources of non-random device mismatch that can impact dense SRAM designs. We also examined two different bit cell topologies and showed that systematic mismatch decreased the margin limited yield. We found that based on our representative set of pushed rules, the type 4 cell layout continues to offer superior density and reduced BL length compared to that of the type 1x cell. For this reason, reduced dimensions required for the competitive SRAM bit cell as scaling continues below 32nm will place increased demands on the alignment and image tolerances required for large scale SRAM arrays.

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References

[1] M. Ishida, T. Kawakami, A. Tsuji, N. Kawamoto, M. Motoyoshi, and N. Ouchi, "A novel 6t-sram cell technology designed with rectangular patterns scalable beyond 0.18 & generation and desirable for ultra high speed operation," in *Proc. International Electron Devices Meeting IEDM '98 Technical Digest*, 6–9 Dec. 1998, pp. 201–204.

[2] T. Jhaveri, V. Rovner, L. Liebmann, L. Pileggi, A. Strojwas, and J. Hibbeler, "Co-optimization of circuits, layout and lithography for predictive technology scaling beyond gratings," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 29, no. 4, pp. 509 –527, april 2010.

[3] F. Arnaud, F. Boeuf, F. Salvetti, D. Lenoble, F. Wacquant, C. Regnier, P. Morin, N. Emonet, E. Denis, J. Oberlin, D. Ceccarelli, P. Vannier, G. Imbert, A. Sicard, C. Perrot, O. Belmont, I. Guilmeau, P. Sassoulas, S. Delmedico, R. Palla, F. Leverd, A. Beverina, V. DeJonghe, M. Broekaart, L. Pain, J. Todeschini, M. Charpin, Y. Laplanche, D. Neira, V. Vachellerie, B. Borot, T. Devoivre, N. Bicais, B. Hinschberger, R. Pantel, N. Revil, C. Parthasarathy, N. Planes, H. Brut, J. Farkas, J. Uginet, P. Stolk, and M. Woo, "A functional 0.69 μm^2 embedded 6T-SRAM bit cell for 65 nm CMOS platform," in *VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on*, 2003, pp. 65 – 66.

[4] F. Boeuf, F. Arnaud, C. Boccaccio, F. Salvetti, J. Todeschini, L. Pain, M. Jurdit, S. Manakli, B. Icard, N. Planes, N. Gierczynski, S. Denorme, B. Borot, C. Ortolland, B. Duriez, B. Tavel, P. Gouraud, M. Broekaart, V. Dejonghe, P. Brun, F. Guyader, P. Morini, C. Reddy, M. Aminpur, C. Laviron, S. Smith, J. P. Jacquemin, M. Mellier, F. Andre, N. Bicais-Lepinay, S. Jullian, J. Bustos, and T. Skotnicki, "0.248&and 0.334&conventional bulk 6t-sram bit-cells for 45nm node low cost - general purpose applications," in *Proc. Digest of Technical Papers VLSI Technology 2005 Symposium on*, 14–16 June 2005, pp. 130–131.

[5] B. Haran, A. Kumar, L. Adam, J. Chang, V. Basker, S. Kanakasabapathy, D. Horak, S. Fan, J. Chen, J. Faltermeier, S. Seo, M. Burkhardt, S. Burns, S. Halle, S. Holmes, R. Johnson, E. McLellan, T. Levin, Y. Zhu, J. Kuss, A. Ebert, J. Cummings, D. Canaperi, S. Paparao, J. Arnold, T. Sparks, C. Koay, T. Kanarsky, S. Schmitz, K. Petrillo, R. Kim, J. Demarest, L. Edge, H. Jagannathan, M. Smalley, N. Berliner, K. Cheng, D. LaTulipe, C. Koburger, S. Mehta, M. Raymond, M. Colburn, T. Spooner, V. Paruchuri, W. Haensch, D. McHerron, and B. Doris, "22 nm technology compatible fully functional 0.1 μm^2 6T SRAM cell," in *Proc. IEEE International Electron Devices Meeting IEDM 2008*, 15-17 Dec. 2008, pp. 1–4.

[6] Z. Luo, A. Steegen, M. Eller, R. Mann, C. Baiocco, P. Nguyen, L. Kim, M. Hoinkis, V. Ku, V. Klee, F. Jamin, P. Wrschka, P. Shafer, W. Lin, S. Fang, A. Ajmera, W. Tan, D. Park, R. Mo, J. Lian, D. Vietzke, C. Coppock, A. Vayshenker, T. Hook, V. Chan, K. Kim, A. Cowley, S. Kim, E. Kaltalioglu, B. Zhang, S. Marokkey, Y. Lin, K. Lee, H. Zhu, M. Weybright, R. Rengarajan, J. Ku, T. Schiml, J. Sudijono, I. Yang, and C. Wann, "High performance and low power transistors integrated in 65nm bulk cmos technology," in *Proc. IEDM Technical Digest Electron Devices Meeting IEEE International*, 2004, pp. 661–664.

[7] S. Ohbayashi, M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Imaoka, Y. Oda, T. Yoshihara, M. Igarashi, M. Takeuchi, H. Kawashima, Y. Yamaguchi, K. Tsukamoto, M. Inuishi, H. Makino, K. Ishibashi, and H. Shinohara, "A 65-nm SoC embedded 6T-SRAM designed for manufacturability with read and write operation stabilizing circuits," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 820–829, April 2007.

[8] S. Hasegawa, Y. Kitamura, K. Takahata, H. Okamoto, T. Hirai, K. Miyashita, T. Ishida, H. Aizawa, S. Aota, A. Azuma, T. Fukushima, H. Harakawa, E. Hasegawa, M. Inohara, S. Inumiya, T. Ishizuka, T. Iwamoto, N. Kariya, K. Kojima, T. Komukai, N. Matsunaga, S. Mimotogi, S. Muramatsu, K. Nagatomo, S. Nagahara, Y. Nakahara, K. Nakajima, K. Nakatsuka, M. Nishigoori, A. Nomachi, R. Ogawa, N. Okada, S. Okamoto, K. Okano, T. Oki, H. Onoda, T. Sasaki, M. Satake, T. Suzuki, Y. Suzuki, M. Tagami, K. Takeda, M. Tanaka, K. Taniguchi, M. Tominaga, G. Tsutsui, K. Utsumi, S. Watanabe, T. Watanabe, Y. Yoshimizu, T. Kitano, H. Naruse, Y. Goto, T. Nakayama, N. Nakamura, and F. Matsuoka, "A cost-conscious 32nm cmos platform technology with advanced single exposure lithography and gate-first metal gate/high-k process," in *Proc. IEEE International Electron Devices Meeting IEDM 2008*, 15–17 Dec. 2008, pp. 1–3.

[9] G. Georgakos, P. Huber, M. Ostermayr, E. Amirante, and F. Ruckerbauer, "Investigation of Increased Multi-Bit Failure Rate Due to Neutron Induced SEU in Advanced Embedded SRAMs," *IEEE Symposium on VLSI Circuits*, pp. 80–81, 2007.

[10] S. Sze, *VLSI technology.* McGraw-Hill New York, 1988.

[11] D. Losee, J. Lavine, E. Trabka, S. Lee, and C. Jarman, "Phosphorus diffusion in polycrystalline silicon," *Journal of Applied Physics*, vol. 55, p. 1218, 1984.

[12] H. Puchner and S. Selberherr, "An advanced model for dopant diffusion in polysilicon," *IEEE Transactions on Electron Devices*, vol. 42, no. 10, pp. 1750–1755, 1995.

[13] T. B. Hook, J. Brown, P. Cottrell, E. Adler, D. Hoyniak, J. Johnson, and R. Mann, "Lateral ion implant straggle and mask proximity effect," *IEEE Transactions on Electron Devices*, vol. 50, no. 9, pp. 1946–1951, Sept. 2003.

[14] Y. Sheu, K. Su, S. Tian, S. Yang, C. Wang, M. Chen, and S. Liu, "Modeling the well-edge proximity effect in highly scaled MOSFETs," *IEEE Transactions on Electron Devices*, vol. 53, no. 11, pp. 2792–2798, 2006.

[15] I. Polishchuk, N. Mathur, C. Sandstrom, P. Manos, and O. Pohland, "CMOS Vt-control improvement through implant lateral scatter elimination," in *IEEE International Symposium on Semiconductor Manufacturing, 2005. ISSM 2005*, 2005, pp. 193–196.

[16] T. Hook, J. Brown, M. Breitwisch, D. Hoyniak, and R. Mann, "High-performance logic and high-gain analog CMOS transistors formed by a shadow-mask technique with a single implant step," *IEEE Transactions on Electron Devices*, vol. 49, no. 9, pp. 1623–1627, 2002.

[17] T. Hook and G. Leak, "Method of selectively adjusting ion implantation dose on semiconductor devices," US Patent 7,682,910, March 23, 2010.

[18] S.-Y. Wu, J. Liaw, C. Lin, M. Chiang, C. Yang, J. Cheng, M. Tsai, M. Liu, P. Wu, C. Chang, L. Hu, C. Lin, H. Chen, S. Chang, S. Wang, P. Tong, Y. Hsieh, K. Pan, C. Hsieh, C. Chen, C. Yao, C. Chen, T. Lee, C. Chang, H. Lin, S. Chen, J. Shieh, S. Jang, K. Chen, Y. Ku, Y. See, and W. Lo, "A highly manufacturable 28nm cmos low power platform technology with

fully functional 64mb sram using dual/tripe gate oxide process," in *VLSI Technology, 2009 Symposium on*, 16-18 2009, pp. 210 –211.

[19] A. Papoulis and S. Pillai, *Probability, random variables, and stochastic processes*. McGraw-Hill New York, 2002.

[20] E. Seevinck, F. List, and J. Lohstroh, "Static-noise margin analysis of mos sram cells," *IEEE Journal of Solid-State Circuits*, vol. SC-22, pp. 748–754, 1987.

[21] J. Wang, S. Nalam, and B. H. Calhoun, "Analyzing static and dynamic write margin for nanometer SRAMs," in *Proc. Int. Symp. on Low power electronics and design*. New York, NY, USA: ACM, 2008, pp. 129–134.

[22] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of mos transistors," vol. 24, no. 5, pp. 1433–1439, Oct 1989.

[23] T. Hook, J. Johnson, J.-P. Han, A. Pond, T. Shimiu, and G. Tsutsui, "Channel length and threshold voltage dependence of transistor mismatch in a 32nm HKMG technology," *IEEE Transactions on Electron Devices*, vol. 57, no. 10, pp. 2440–2447, 2010.

[24] J. B. Johnson, T. B. Hook, and Y.-M. Lee, "Analysis and modeling of threshold voltage mismatch for cmos at 65 nm and beyond," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 802–804, July 2008.

[25] S. Bordez, A. Cathignol, and K. Rochereau, "A continuous model for mosfet vt matching considering additional length effects," in *Proc. IEEE International Conference on Microelectronic Test Structures ICMTS '07*, 19–22 March 2007, pp. 226–229.

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