High-Performance Logic and High-Gain Analog CMOS Transistors Formed by a Shadow-Mask Technique With a Single Implant Step

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***Abstract*—Transistors have been fabricated with a photoresist mask placed in close proximity to the gate so as to effectively block the angled halo implant from the gate region. Devices for which the halo has been eliminated demonstrate superior drain conductance, while devices with the halo implant show the short-channel effect required for high performance. Asymmetric devices have also been fabricated in a similar manner, producing devices with improved analog characteristics without an additional masking layer.**

***Index Terms*—Analog integrated circuits, CMOSFETS.**

I. Introduction

THE HALO or pocket implant is a key aspect to controlling the threshold voltage in short-channel transistors [1]. An implant of the same type as the well doping is done after the formation of the gate conductor and generally at the same time as the extension or lightly doped drain (LDD) implant. Because the implant is blocked from the channel region by the gate polysilicon, the average doping concentration under the gate increases as the channel length gets shorter thereby mitigating the short-channel threshold roll-off. Often the halo implant is done at an angle with respect to wafer; this can aid in placing the implant under the gate and not under the source/drain implant, where it increases the junction capacitance. There are important limitations to the use of the halo. The halo causes an increase in threshold voltage at shorter channels (sometimes known as the reverse short channel effect [RSCE]) [2], particularly when measured at low drain bias. This can reduce the current drive for all but the shortest devices. In general, more highly scaled transistors (i.e., lower power supply, shorter channels, thinner gate oxide) tend to have higher halo doses than higher voltage transistors. The large electric field associated with high halo doping is unacceptable for operation at high voltage because of hot-carrier concerns and premature breakdown. Finally, the halo is disadvantageous for devices operated as a linear amplifier inasmuch as the output conductance is degraded for devices with a halo implant [3]–[5]. Therefore, it is desirable to be able to provide devices with varying amounts of halo dose on the same wafer: short-channel transistors with large drain bias need a large halo dose to control the short-channel effect; high-voltage transistors require less halo dose; transistors operating in an analog fashion also require little or no halo dose.

It is a relatively simple matter to provide a multiplicity of masking levels and implants to accomplish all these goals on the same wafer, but it is obviously advantageous to be able to accomplish them simultaneously with the same masking step and implant sequence. In this paper, we describe such a method and show data on symmetric halo and haloless devices, and also devices built with a halo on one side and not the other. All of these devices were fabricated with noncritical mask alignment by utilizing the shadow-mask technique described in the following.

By blocking the halo implant, an improvement in transistor self gain (gm/gds) of as much as a factor of ten is demonstrated, and undesirable threshold voltage rollup was completely eliminated.

II. Shadow-Mask Technique

As mentioned earlier, it is not uncommon that the halo implant is performed at an angle with respect to the wafer normal. The angle can help to place the halo implant where desired: between the source and the drain and not below the drain. This is schematically illustrated in Fig. 1, where the extension, halo, and source/drain contours are indicated for representative steep- and shallow-angle halo implants.

If the halo implant is designed for a substantial angle from the normal, then the standard mask in place at that time can be used to shadow the halo implant from a particular gate. The placement of the mask has wide latitude, as the thickness of the photoresist and the angle of the implant determines the length of the shadow. Fig. 2 shows the manner in which the angled halo implant is shadowed by the resist. For a typical process in which the halo and extension implants are done with the same mask, there are two constraints on the location of the mask edge relative to the gate. The minimum distance that the gate may be from the edge of the resist is determined by the requirement that adequate extension implant be implanted to link up under the spacer with the deep source/drain implant. The maximum distance that the resist may be from the gate is the thickness of the resist multiplied by the tangent of the implant angle with respect to the normal $-t^* \tan(\phi)$ in Fig. 2. A typical resist thickness of about 0.5 μm and an implant angle of 45° allows approximately 0.4 μm of alignment and image-size tolerance, which is a simple matter to achieve with modern processes. Fig. 3 shows how a device may be successfully fabricated even with worst-case misalignment.

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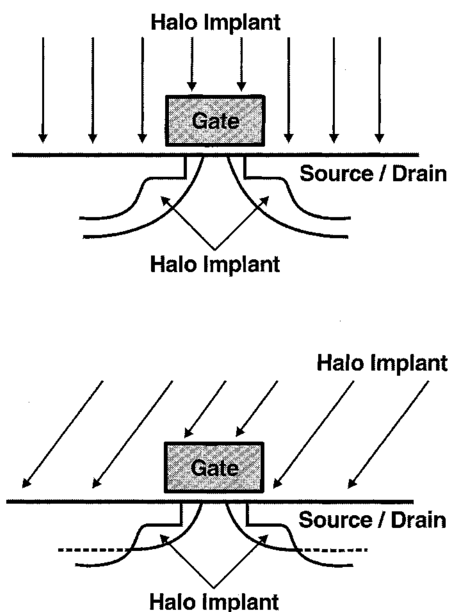

Fig. 1. Schematic illustration of halo placement as a function of implant angle. Upper figure: halo implant angle normal to wafer surface. Lower figure: halo implant at an angle ϕ with respect to the normal.

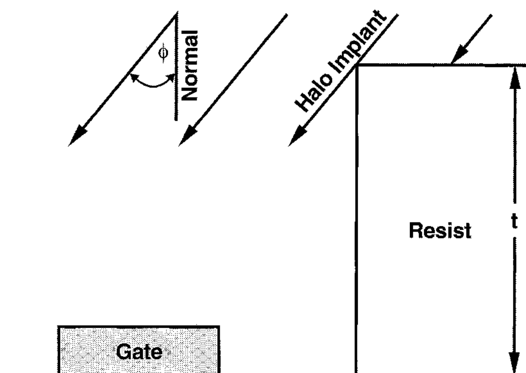

Fig. 2. Schematic illustration of halo shadowing technique.

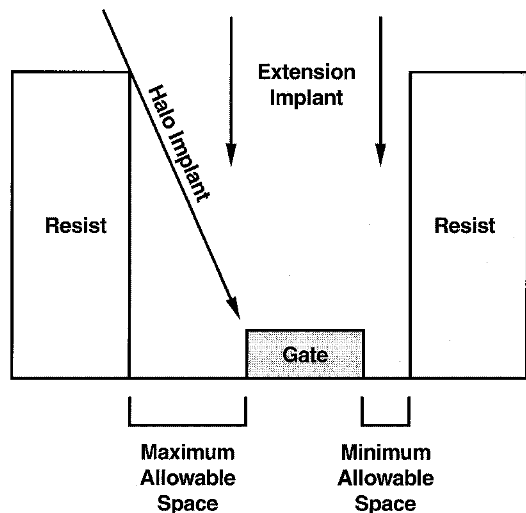

Fig. 3. Schematic illustration of shadowed device with worst-case mask misalignment.

Of course, the angled implants are performed four times, once for each orientation. The shadowed device receives three of the four rotations, but the most relevant implant is blocked. The data in this paper show that only the implant protruding under the gate plays an important role in determining the electrical characteristics.

For these experiments, a set of test structures were designed to simultaneously create four types of devices: thin oxide devices with halo implants, thick oxide devices with the same halo implants, thick oxide devices with the halo implants blocked by the shadow technique, and asymmetric devices with one side blocked and the other side with a halo.

Different channel lengths were provided for each device type to fully characterize the effect.

III. Experimental Results

The process used in these experiments was a 0.18-μm shallow-trench isolated CMOS technology with copper metallurgy and two gate-oxide thicknesses. The thin gate-oxide devices have oxide thickness of 2.9 nm, with polysilicon gate length of 135 nm intended for usage at 1.5 V. The devices with 5.2-nm oxide have a polysilicon gate length of 240 nm and are targeted for 2.5 V IO applications. An adaptation of a standard 0.18-μm technology [6], both sets of devices have a relatively high threshold voltage for reduced leakage and portable applications. Conventional bulk silicon wafers, dual workfunction polysilicon, silicon nitride spacers, and self-aligned cobalt silicide further define the important technology elements.

Extension and halo implants appropriate to the thin oxide 1.5 V devices were designed. For these devices adequate threshold voltage is maintained down to the shortest allowed channel length. The use of the same implants in the thick oxide device, however, results in an excessively large threshold voltage at the nominal channel length of this device. By blocking the halo implant with the shadow mask, the target threshold voltages at nominal channel length are achieved. Figs. 4 and 5 show the threshold voltage as a function of channel length for devices with and without the halo block image (for nfet and pfet, respectively). The desired specifications for channel length and threshold voltage for this application are indicated in the figures. Further optimization of the devices may be accomplished by providing a portion of the halo dose at an angle of zero degrees (that will be implanted into both devices) and a portion at a shallower angle (that will be blocked by the shadow mask).

The transistor gain characteristics were also measured. A set of I_d–V_d curves for a representative shadowed and unshadowed thick oxide device are shown in Fig. 6. The reduction in drain conductance for the shadowed case is clearly evident. For shorter channel devices, the drain-induced barrier lowering (DIBL) effect dominates, and the drain conductance of the shadowed device degrades rapidly. Additional data were taken on a variety of design lengths so that the optimum channel length could be determined. The transconductance (gm) was also measured as $\Delta I_{ds}/\Delta V_g$ and the drain conductance (gds) as $\Delta I_{ds}/\Delta V_d$. An operating point of 300 mV of gate overdrive and a drain voltage of 2 V was chosen to characterize the gain. The device self gain was calculated as gm divided by gds. The results of these measurements and calculations are shown in

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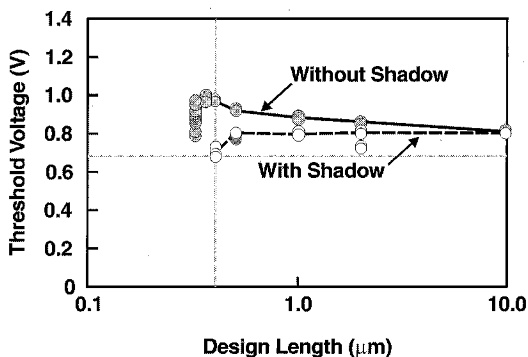

Fig. 4. Saturated threshold voltage for 2.5-V thick-oxide nFETs as a function of channel length with and without the halo-block mask image.

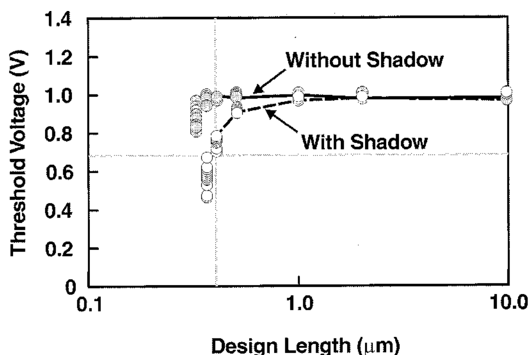

Fig. 5. Absolute value of saturated threshold voltage for 2.5-V thick-oxide pFETs as a function of channel length with and without the halo-block mask image.

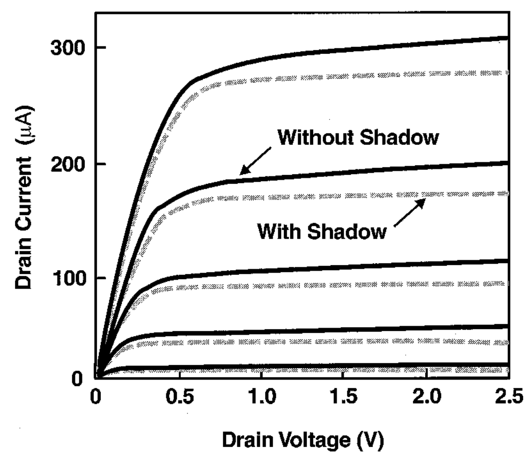

Fig. 6. I_d–V_d curves for shadowed and unshadowed 5.2-nm devices. Each curve is taken for a similar gate overdrive. Design channel lenght is 2.0 μm.

Figs. 7 and 8, for nFETs and pFETs, respectively. For channel lengths larger than 0.5 μm, the self gain of the shadowed device is clearly superior, while the halo device is better for the shorter channel lengths. As described earlier, both types of devices are formed simultaneously simply by the addition of a nearby blocking image.

It is also a simple matter to form an asymmetric device with the halo shadowed on only one side. We have characterized the self gain of these asymmetric devices operated in both the forward and reverse mode. We define the forward mode as the one in which the side with the halo blocked out is considered to be the drain side. For these plots the operating point is still with gate voltage at 300 mV above threshold, but the drain voltage was 1 V. The data for nfet and pfet are represented in Figs. 9 and 10, respectively, superimposed upon the results for a fully shadowed and a completely unshadowed

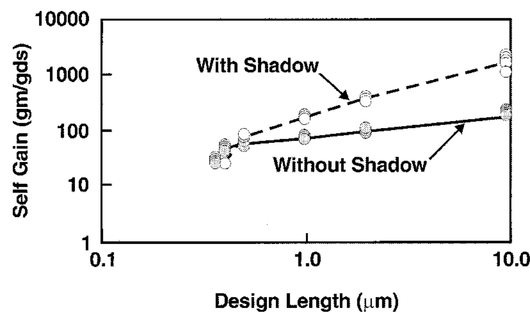

Fig. 7. Self gain as a function of channel length for shadowed and unshadowed 5.2-nm nFETS.

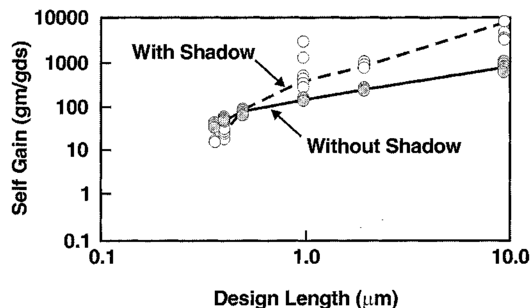

Fig. 8. Self gain as a function of channel length for shadowed and unshadowed 5.2-nm PFETs.

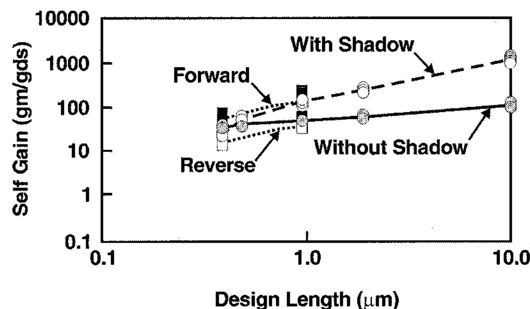

Fig. 9. Self gain as a function of channel length for shadowed, unshadowed, and asymmetric 5.2-nm NFETs. Symmetric devices are indicated by circles, asymmetric with squares. Asymmetric devices were measured in both forward (solid) and reverse (open) mode.

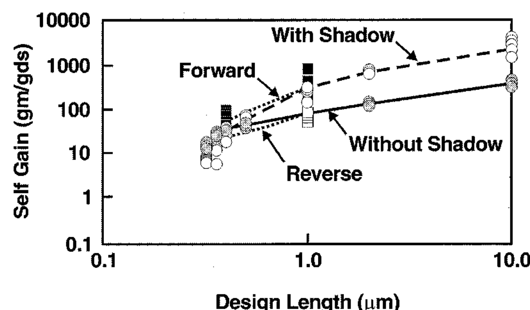

Fig. 10. Self gain as a function of channel length for shadowed, unshadowed, and asymmetric 5.2 nm PFETs. Symmetric devices are indicated by circles, asymmetric with squares. Asymmetric devices were measured in both forward (solid) and reverse (open) mode.

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TABLE I
SELF GAIN FOR THIN-OXIDE DEVICES OF TWO DIFFERENT CHANNEL LENGTHS

Channel Length	NFET		PFET	
	Forward	Reverse	Forward	Reverse
0.18μm	16.3	13.6	10.9	10.2
1.00 μm	243.0	40.0	347.0	113.0

set of devices. The asymmetric devices operated in reverse resemble the unshadowed devices; in both cases, there is a halo situated at the drain side of the junction, which degrades the output conductance. For the asymmetric devices operated in the normal manner, with a halo implant only at the source side of the device, the advantages become apparent. The asymmetric device with a relatively long 1-μm channel length looks nearly identical to the fully shadowed device, but the performance of the shorter-channel device is clearly superior. These benefits are realized because there is no halo on the drain side to degrade the conductance, but there is a halo on the source side to reduce and control DIBL.

The same techniques may be applied to the thin oxide devices to obtain superior analog performance. Table I summarizes the self gain of the thin oxide devices for two different channel lengths. Superior analog performance is readily realized for the longer channel length devices by the addition of the shadow mask on the appropriate side of the device. The shorter channel devices are not very asymmetric because the source is so close to the drain, and the implant regions overlap.

In the experiments reported here, the halo angle was 45° and the shadow mask placed at a distance appropriate to this angle. Variations in mask alignment and thickness did not affect the electrical results. In another set of experiments with a halo implant at 30° from the normal and the same mask set, a large variability in electrical results was noted, as the variations in masking sometimes blocked the implant and sometimes did not. It is important to apply the considerations indicated in Fig. 3 to define the proper layout rules for a robust process.

IV. CONCLUSION

We have shown how a variety of devices may be obtained simultaneously at no additional cost by selectively blocking the halo implant from one or both sides of the transistor by shadowing the implant. This technique is made possible by using a shallow-angle halo implant (typically from 30° to 45° from the normal). The shadowed devices were shown to have the short-channel effect typical of devices without a halo implant and also superior analog performance (i.e., transistor self gain) at relatively long channel lengths of 0.5 μm or more. An optimum device with better self gain across the entire length spectrum was shown in an asymmetric device, where the halo was shadowed only on the drain side.

The shadow mask alignment requirements are not prohibitive, as the tolerance is effectively magnified by the halo implant angle. To fully realizing the benefits of the shadow technique, the halo implant must be defined at an angle sufficient to enable the block mask placement to be achievable within the normal alignment parameters.

Detailed optimization may be done by introducing a multiplicity of halo implants, some blocked and others not. We also note that the extension implant, or a portion thereof, can also be adapted for this technique. In a manner analogous to the asymmetric halo devices described above, it is generally desirable to eliminate the LDD implant from the source side of a transistor, which may be accomplished if the LDD implant is done at a sufficient angle with respect to the normal.

This powerful technique is readily extendible into the 0.13-μm and 0.10-μm technology nodes and offers superior mixed signal capability with no additional process complexity. To fully realize the advantages of the asymmetric device, the circuit and layout must distinguish the source from the drain, which may require additional modeling and design infrastructure.

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