Noise Margin and Leakage in Ultra-Low Leakage SRAM Cell Design

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Abstract—**Various aspects of ultra-low leakage static random-access memories (SRAM) cell design are considered. It is shown that the high threshold voltage relative to the power supply so improves the stability of the cell that the beta ratio of the design may be made very small for improved performance. Also, the ramifications of threshold uncertainty due to random dopant fluctuations are investigated, and it is shown that chip performance will be adversely affected by this phenomenon.**

Index Terms—**CMOSFETS, CMOS memory integrated circuits, random access memory (RAM).**

I. Introduction

The ultra-low leakage regime (<50 fA/cell at room temperature) for static random-access memories (SRAM) designs imposes unique constraints on the cell design, in many ways different from those imposed by performance-driven scaling concerns. Cell size is of paramount importance regardless of the device threshold voltage, but beyond that the similarity ends. The high threshold voltage associated with the ultra-low leakage design point provides substantial relief to the static noise margin (SNM) for a given design, but the intrinsic threshold variation limits the performance available from the cell. The intrinsic threshold variation affects the leakage as well, but in a less significant manner.

To achieve ultra-low leakage specs on the order of 50 fA/cell, the threshold voltage must be on the order of 700 mV or more, and to maintain reasonable performance, the nominal power supply is typically 1.5 to 1.8 V. In contrast, the high-performance roadmap technology node of 0.13 μm has a power supply of 1.2–1.5 V and a threshold voltage on the order of 350 mV. Gate leakage restricts the oxide thickness of ultra-low leakage SRAMs to 2.7–3.0 nm, while performance-oriented 0.13-μm technologies have gate oxide 1.7–2.2 nm in thickness. Gate-induced drain leakage (GIDL) considerations may limit the junction design for ultra-low leakage technologies, whereas high-performance device design is not so constrained. The absolute value of the threshold and the performance is quite different for these design points; therefore the SRAM cell design and constraints will also be very different.

In this brief, we report on calculations and measurements of SNM, performance, and leakage for 0.18 and 0.13-μm ultra-low power SRAM cell designs.

II. Static Noise Margin (SNM)

The static noise margin is a measure of the cell's ability to retain its data state. The worst-case situation is usually under "read-disturb" conditions. When the wordline device is turned on and connects the precharged bitline to the low side of the cell the state of the cell may flip if the internal node voltage rises to a high enough level. The problem is exacerbated if the ratio of the conductances of the pulldown and the wordline devices (often called beta) is too small. Mismatch in devices between the left and right side of the cell also degrades the noise margin, but will not be directly addressed in this section. A means of analyzing the SNM is provided by an examination of the cell's "butterfly curve" as in Fig. 1. In this figure, the left internal node voltage is plotted against the right internal node voltage, for a sweep from left-to-right and then from right-to-left. The difference between the two curves, or the hysterisis, (as indicated on Fig. 1) is a measure of the stability of the cell. For the purposes of this paper we define the static noise margin, in units of mV, as the longest vector between the two curves.

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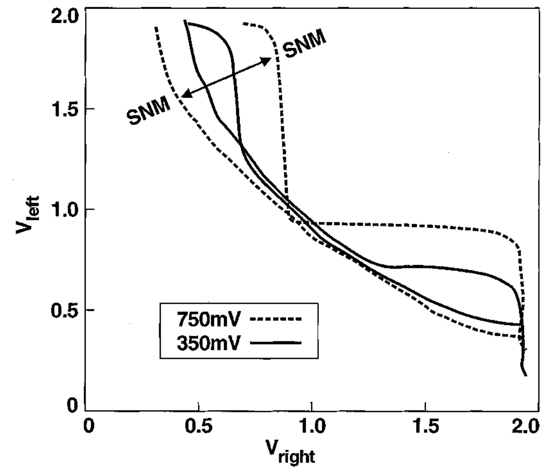

Fig. 1. Illustration of butterfly curve and static noise margin. Simulated butterfly curves for cells with two different threshold voltages. The vertical axis is the voltage on the left cell node, and the abscissa is the voltage on the right cell node dotted lines: $V_t = 750$ mV; solid lines: $V_t = 350$ mV.

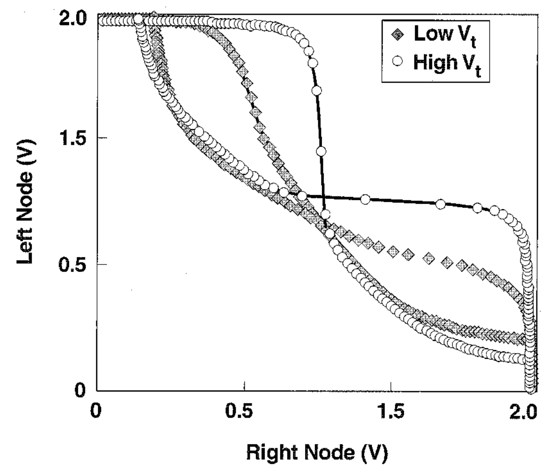

Fig. 2. Experimental butterfly curves for high and low threshold voltage devices. Solid diamonds: low V_t (~300 mV); open circles: high V_t (~700 mV).

For a given cell design, higher threshold devices will make the cell more stable. To flip the cell, the internal node on the low side needs to rise to a threshold or more. This will virtually never happen when the threshold is larger than half the power supply; hence the cell is extremely stable for the ultra-low power design point, regardless of the beta in the design. Fig. 1 shows simulated butterfly curves for the same cell physical design, using devices with different threshold voltages. In Fig. 2 measured curves for devices with widely different thresholds are shown, and the reduction in noise margin for the lower threshold is evident.

To generalize the conclusions, we have simulated the SNM as a function of $V_{\rm dd}$ for a variety of 0.13-μm technology design points. Noise

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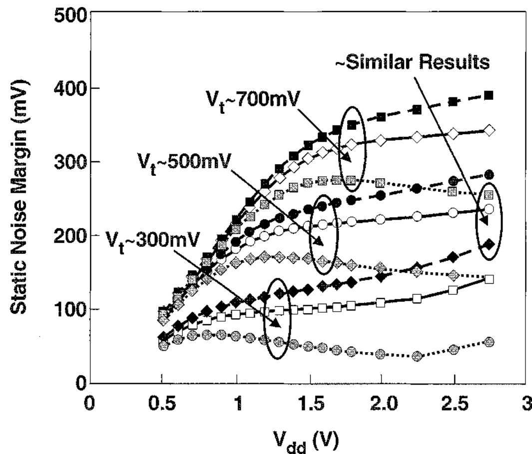

Fig. 3. Simulated SNM as a function of V_{dd} for various threshold voltages and cell beta. Shaded symbols: cell beta = 1. Open symbols: cell beta = 1.5. Filled symbols: cell beta = 2.

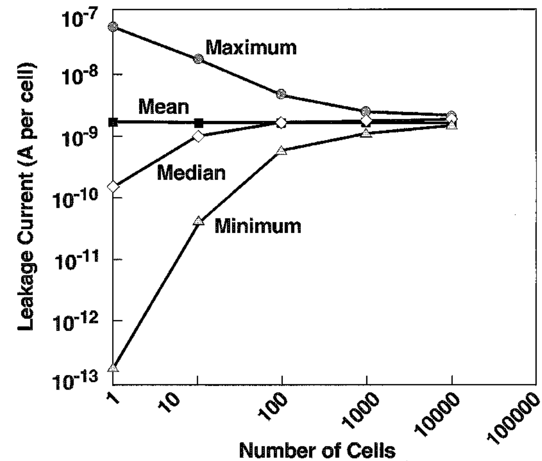

Fig. 4. Statistical model of leakage in amperes at 85°C for increasing number of cells. Uncertainty = 160 mV (3-sigma). Some cells have very low leakage, some cells have higher leakage. The overall leakage is considerably different than would be predicted from the leakage of a single cell.

margin for three different betas was calculated; beta was changed by varying the wordline device width, keeping the other device dimensions constant. For this specific layout, it was possible to vary the wordline width without varying the overall cell size. The same cell designs were assessed for various performance technology points by varying the threshold voltage. The ultra-low leakage design point was represented by devices with threshold voltage of approximately 700 mV, the high-performance design point with threshold voltage of approximately 300 mV, and the leakage/performance tradeoff point with a threshold voltage halfway between these two points. We have run the simulation up to 2.5 V for illustrative purposes, and also to represent burn-in or extreme stress conditions.

All nine of these simulated curves are represented in Fig. 3. For low V_{dd} the SNM increases linearly with V_{dd} as the low is held ever more firmly low by increasing gate drive on the pulldown device. However, at higher V_{dd} the noise margin levels off and may even decrease. This occurs when V_{dd} is approximately twice the threshold voltage. Below that point the source-follower voltage drop across the wordline device prevents the internal node voltage from approaching the threshold voltage needed to flip the cell. Above that voltage the potential on the node depends on the beta ratio. For each threshold voltage it is apparent from the figure that the higher beta cell design is more stable. However, high threshold voltage confers such a large noise margin on the cell so that the cell with beta of one with high-V_t devices is more stable than the cell with beta of two with low-V_t devices. In Section III, we will discuss the advantage of designing a low-beta cell for ultra-low power application.

III. Performance

In some sense, writability and read access time is the obverse of stability. The more stable the cell the more difficult it will be to write the cell into a different state. As indicated above, a cell design with a narrower wordline device is more stable, but as the current through such a device is smaller, it will require more time to develop a signal of a given magnitude on the bitline. The rate at which the cell can pull down the bitline is limited by the series combination of the pulldown device and the wordline device, and is increased by increasing the conductance of either or both devices. (The relative importance of the two devices to the read current is a consequence of the details of the device design and the operating conditions, and may not be precisely equal.) For minimum read delay the widths of both devices should therefore be as wide as possible. In practice, the cell size and the desired beta ratio limits the size of the devices. For an ultra low-power SRAM design, the threshold voltage is high, and the device drive current is correspondingly low, so the read delay in the cell is particularly critical. However, the improved stability associated with higher threshold voltage relieves the constraint of the beta ratio, so the wordline device may be as wide as physically reasonable, even if the resultant beta is less than one.

IV. Cell Leakage, Cell Performance, and Threshold Voltage Uncertainty

For high-performance SRAMs the size-dependent threshold voltage uncertainty significantly reduces the SNM [1]. For ultra low-power SRAM the noise margin is more than adequate, but read performance and leakage current are of foremost importance. With respect to the read performance a single cell can limit the functionality of the chip. There is also an effect on the leakage but the influence of excessively leaky cells is somewhat mitigated by averaging.

Although at room temperature gate leakage or gate-induced drain leakage (GIDL) may dominate the overall leakage of the cell, at elevated temperature it is the threshold voltages of the cell devices that determine the leakage current. A variation of 85 to 100 mV in threshold voltage causes a change of a factor of ten in leakage current; therefore the leakage current in different cells may easily differ to this degree. The leakage current of the array as a whole is the sum of the ensemble of cells, which is larger than the leakage of a median single cell because of the threshold uncertainty. Fig. 4 shows the result of a Monte Carlo simulation of the current of an array of cells represented on a per-cell basis. For only one cell there is a large spread of values; as more cells are averaged into the ensemble the median value of leakage (per cell) increases, but the distribution is tighter. The median changes little for ensembles of more than 1000 cells. Simulations were performed for other values of threshold uncertainty, and Fig. 5 summarizes the array leakage as a function of the threshold voltage uncertainty.

For ultra-low power SRAMs the threshold voltage is usually closer to the nominal power supply than for high-performance designs, and therefore the threshold voltage uncertainty has a proportionately larger impact on the device on-current. As mentioned earlier, if even a single cell fails to develop adequate signal within the time allotted, the chip as a whole will fail to function. Fig. 5 shows the median array leakage and the relative performance impact as a function of threshold voltage uncertainty, expressed in terms of mismatch. In this figure, performance is defined as the read current normalized to a nominal cell. In the ab-

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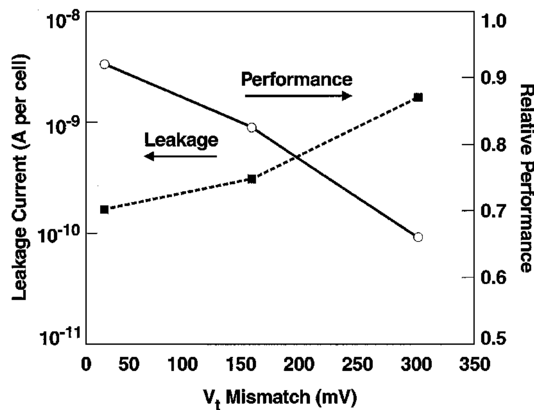

Fig. 5. Median cell leakage in amperes at 85°C and relative performance as a function of threshold uncertainty. The uncertainty is larger for the smaller devices in more advanced technologies.

sence of substantial threshold uncertainty the on-current of the (statistically) slowest device on a given chip is 92% that of the nominal device. For a larger uncertainty in threshold voltage, any particular cell may have only 82% of the nominal current, and for even larger uncertainty, the current may be only 66% of the nominal cell. As the chip must be timed to accommodate the slowest cell, the intermediate point described previously represents an additional 10% loss of performance for the chip overall. For that same amount of threshold uncertainty the overall leakage is approximately twice that of a nominal cell. This is the point most appropriate to the 0.13-μm generation.

As device sizes shrink from the 0.13-μm to the 0.10-μm generation, the uncertainty effect will worsen by a factor of the square root of two, to a value of more than 200 mV. Both leakage and performance will suffer as a consequence.

V. Conclusions

Various characteristics of an SRAM cell design have been investigated with respect to ultra-low leakage applications and some unique aspects have been identified. For the design of an ultra-low leakage cell device, the threshold voltage must be high enough to satisfy the leakage requirements. The wordline device width should be as wide as possible almost without regard to cell stability. The large threshold voltage with respect to the power supply makes the ultra-low power cell exceptionally stable, even with a cell beta of unity or less. Designing a cell with low beta enables optimum performance, which is important where the performance is so limited. The variation in threshold voltage due to stochastic variations was shown to have an important effect on the performance achievable with the ultra-low power cell. A loss of 10% and a doubling of the leakage current were the estimated effects on a cell of the 0.13-μm generation. The impact will be larger in the 0.l0-μm generation, but the strict leakage requirements constrain the threshold voltage to be large and therefore, the cell stability will remain robust.

References

[1] A. Bhavnagarwala *et al.*, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," *IEEE Trans. Electron Devices*, vol. 36, pp. 658–665, Apr. 2001.

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