High Performance and Low Power Transistors Integrated in 65nm Bulk CMOS Technology

Z. Luo, A. Steegen, M. Eller, R. Mann, C. Baiocco, P. Nguyen, L. Kim, M. Hoinkis, V. Ku, V. Klee[3], F. Jamin, P. Wrschka, P. Shafer, W. Lin[2], S. Fang, A. Ajmera, W. Tan[2], D. Park, R. Mo, J. Lian[3], D. Vietzke[3], C. Coppock, A. Vayshenker, T. Hook, V. Chan, K. Kim[3], A. Cowley, S. Kim[3], E. Kaltalioglu[3], B. Zhang[2], S. Marokkey[3], Y. Lin, K. Lee[1], H. Zhu, M. Weybright, R. Rengarajan, J. Ku[4], T. Schiml[3], J. Sudijono[2], I. Yang, Clement Wann

IBM Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY 12533,
[1]IBM Research, Yorktown Heights, NY 10598
[2]Chartered Semiconductor Manufacturing, [3]Infineon Technologies AG, [4]Samsung Electronics Co., Ltd

Abstract

This paper reports a cutting-edge 65nm CMOS technology featuring high performance and low power CMOS devices for both general and low power applications. Utilizing plasma nitrided gate oxide, off-set and slim spacers, advanced co-implants, NiSi and low temperature MOL process, well designed NMOSFET and PMOSFET achieved significant improvement from the previous generation, especially PMOSFET has demonstrated an astonishing 35 % performance enhancement from the previous technology node.

Introduction

65nm bulk CMOS technology described in this paper is targeted for logic, SRAM, mixed signal and mixed voltage I/O applications. It is also a platform for embedded DRAM applications. The devices in this technology achieve excellent balance between performance and power consumption. CMOS devices with three oxide thicknesses are offered in both base (general purpose) and low power technologies to support multiple voltage operation. Low leakage ultra-thin gate oxide and many new technology features enable the base CMOS transistors to cover a wide range of off-state leakage currents, from 0.5nA to 50nA, which satisfy both low power and high performance application. PMOSFET has demonstrated an astonishing 35 % performance enhancement from the previous technology node [1]. Using advanced co-implants, good Vt-roll off control with slim spacer has been demonstrated as well.

Key Process and Technology Features

Fig. 1 reveals the cross section of a 43 nm MOSFET. Table 1 shows the key pitch sizes for this 65nm technology supporting a 0.7x shrink from the previous technology node [1]. Line width control is achieved by using advanced lithography techniques. Good N+ to N-well and P+ to P-well isolation down to 75 nm spacing have been demonstrated with 3500 Å deep STI and retrograde well design. NiSi combined with a low thermal budget middle of line process are essential to control short channel effects and to prevent dopant de-activation. This technology utilizes an advanced low-k BEOL integration scheme (Fig. 2) and offers up to 10 levels of interconnect, 9 levels with copper. The low-k dielectric is extended from the 90nm technology generation offering maximum manufacturing compatibility while maintaining performance. PECVD is utilized to deposit the low-k SiCOH dielectric film.

Table 1 65 nm Technology Key Pitches

Technology	**65 nm Base** Width/Pitch [um]	**65 nm LP** Width/Pitch [um]
RX pitch [um]	0.09/0.20	0.09/0.20
PC min pitch [um]	0.06/0.20	0.08/0.22
CA pitch [um]	0.09/0.195	0.09/0.195
M1 pitch [um]	0.09/0.18	0.09/0.18
Vx pitch [um]	0.10/0.20	0.10/0.20
Mx pitch [um]	0.10/0.20	0.10/0.20
SRAM [um2]	0.51-0.625	0.52-0.68

Device Design

Historically, aggressive scaling of gate oxide thickness was one of the key methods to improve device performance. However, the high gate leakage current through ultra-thin gate oxide increases stand-by power significantly. Moreover, it becomes the limiting factor of the offering of a high Vt and low leakage device. Therefore, gate oxide for base CMOS devices described here is targeted at 12.5 Å to balance the performance and power consumption. The performance metrics of device offering summarized in Table 2 reflects this design philosophy. The three thin oxide devices cover a wide range of the off-state currents, from 0.5nA to 50nA, which greatly satisfy the needs of SoC applications. Moreover, we offer an additional low leakage flavor in this technology with low power devices, with gate leakage less than 30 pA/μm and GDIL lower than 10 pA/μm.

0-7803-8684-1/04/$20.00 ©2004 IEEE

Table 2 65 nm Base and LP Device Offering

	65 nm Base Device			65 nm LP Device		
	HVT	RVT	LVT	HVT	RVT	LVT
Vdd (V)	1.0			1.2		
Tox (nm)	1.25			1.8		
Ldes (nm)	60			80		
Lpoly (nm)	43			55		
Vt (V)	0.36 / 0.34	0.28 / 0.25	0.19 / 0.15	0.5 / 0.46	0.38 / 0.34	0.26 / 0.22
Ion (uA/um)	560 / 280	695 / 360	830 / 435	460 / 195	600 / 275	725 / 365
Ioff (nA/um)	0.5	5	50	0.01	0.3	7
I/O Devices	Base Technology support 1.5 V and 2.5 V I/O devices LP Technology support 1.8 V and 2.5 V I/O devices					

Base Devices

(1) Gate Oxide: A 12.5 Å plasma nitrided gate oxide is the key to achieve high drive current and low gate leakage current. Through optimized gate oxide process, poly-gate dopant engineering and low temperature MOL process to reduce dopant deactivation, we have achieved Tinv of 19Å/20Å (Fig. 3) with low gate leakage current for NMOSFET/PMOSFET on this 12.5 Å gate oxide. Good oxide reliability (Fig. 4), excellent NBTI and hot carrier properties have also been demonstrated.

(2) Spacer-Junction Engineering: An off-set spacer is used for halo-extension implants. A difference of spacer thickness between NMOSFET and PMOSFET is deliberately created to balance the NMOSFET/PMOSFET performance and short channel effects. A slim spacer is used for S/D implant to reduce series resistance and improve device performance. Moreover, the slim spacer fits better with the aggressive ground rule at this technology node. However, a slim spacer causes degraded short channel effects, especially for PMOSFET. In order to solve this challenge, advanced co-implants are used to control dopant diffusion. As shown in Fig. 5, using advanced co-implants [2] for both NMOSFET and PMOSFET, better or comparable Vt roll-off are achieved even with a 200 Å smaller spacer. Retrograde channels, low energy and high angle halo implants, and shallow extension implants coupled with advanced co-implants and proper spike anneal to control dopant diffusion result in well controlled short channel effects down to 35 nm.

(3) Device Performance: Fig. 6 and Fig. 7 show the typical Id-Vds and Id-Vg for LVT NMOSFET and PMOSFET with 43 nm gate length. Both NMOSFET and PMOSFET show excellent drive current: 830/435 μA/μm at Ioff=50nA/μm at |Vds|=|Vgs|=1.0V, respectively. Sub-threshold slope is about 90 mV/dec for both devices. Drive currents at 1130/610 μA/μm for NMOSFET/PMOSFET can be achieved at 1.2V overdrive while still maintain good sub-threshold characteristics. Fig. 8 shows the representative drive current vs. off-state current of both NMOSFET and PMOSFET at operation voltage of 1V. The PMOSFET's drive current is among the best reported to date with similar device dimension [3-6].

LP Device

An 18Å heavily nitrided gate oxide enables us to limit gate leakage less than 30pA/μm at the operating voltage of 1.2V (Fig. 9) and still achieve high performance. High angle and low dose halo implants results in reduced junction and GIDL leakage while still maintain good short channel effects. Both NFET and PFET have achieved GIDL less than 10pA/μm. Similar to base devices, advanced co-implants are used to control dopant diffusion for slim S/D spacer. The devices with a nominal gate length of 55nm show good Vt-roll-off down to 45nm (Fig. 10). And good output and sub-threshold characteristics have been demonstrated as shown in Fig. 11 and Fig. 12.

SRAM

A range of SRAM cell sizes from 0.51 to 0.68μm^2 are provided for this technology which are optimized for density, performance or low power. All cell options are split word line designs and are compatible (common up to M1) with M2 or M3 bit line design options. A top down SEM (Fig. 13) shows the standard and shared contact configuration in the 0.51μm^2 cell with the insulation stripped away. The butterfly curves for the 0.625μm^2 cell are shown in Fig. 14.

Conclusion

The state-of-the-arts CMOS transistors are presented together with key features in 65 nm bulk CMOS technology. In this leadership technology, both base and low power NMOSFET/PMOSFET achieve high drive current while maintaining low leakage current and good Vt roll-off.

Acknowledge

The authors would like to thank Scott Crowder and Lisa Su for their support of this work.

References

[1] S. F. Huang et al., IEDM 2001, pp. 237-241
[2] K. L. Lee et al., IEDM 2003, pp. 481-484
[3] Y. Nakahara et al., IEDM 2003, pp. 281-284
[4] S. Thompson et al., IEDM 2002, pp. 61-64
[5] K. Goto et al., Symp. VLSI Tech. 2003, pp. 49-50
[6] S. Fung et al., Symp. VLSI Tech. 2004, pp. 92-93

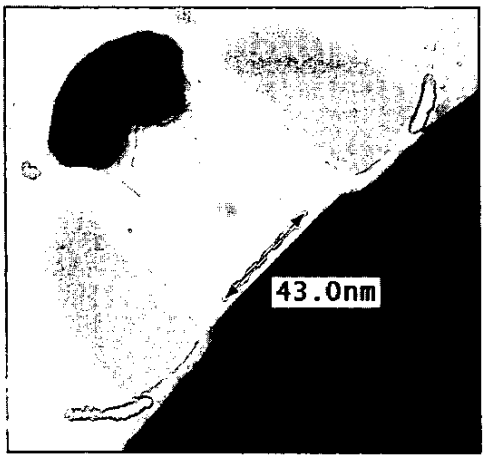

Fig. 1 Cross Section of a 43 nm Transistor

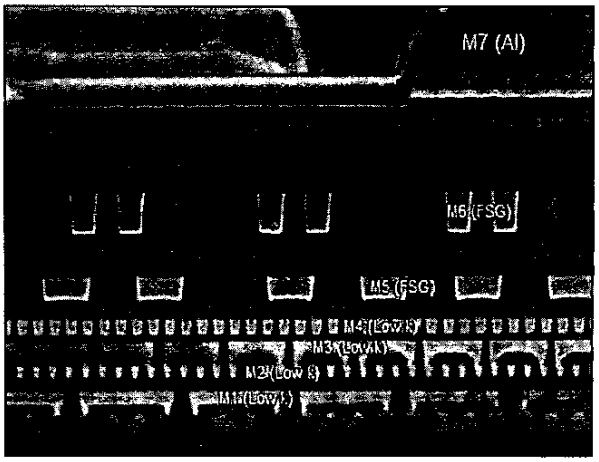

Fig. 2 Cross Section of BEOL

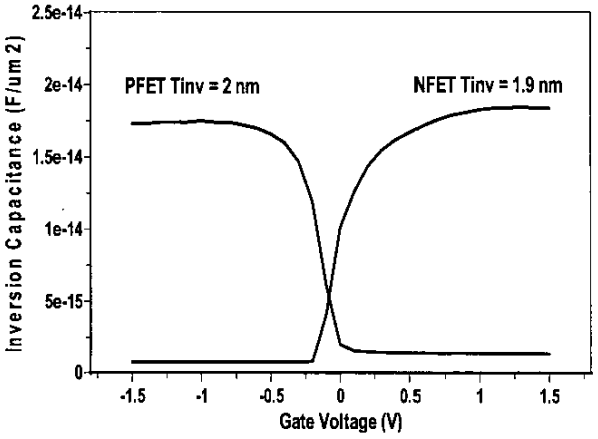

Fig. 3 Inversion Capacitances of 12.5Å Gate Oxide

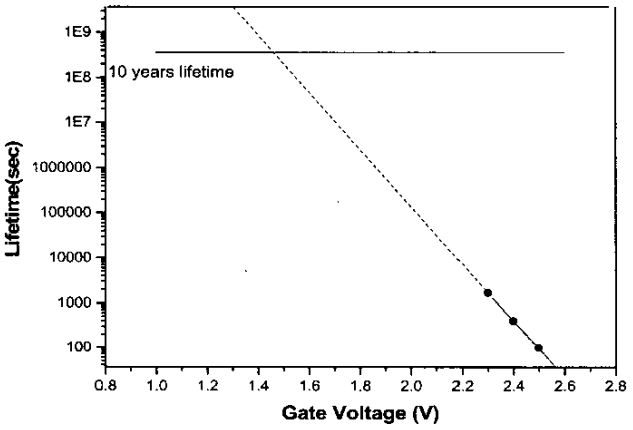

Fig. 4 Life Time Projection for Gate Oxide of Base Device

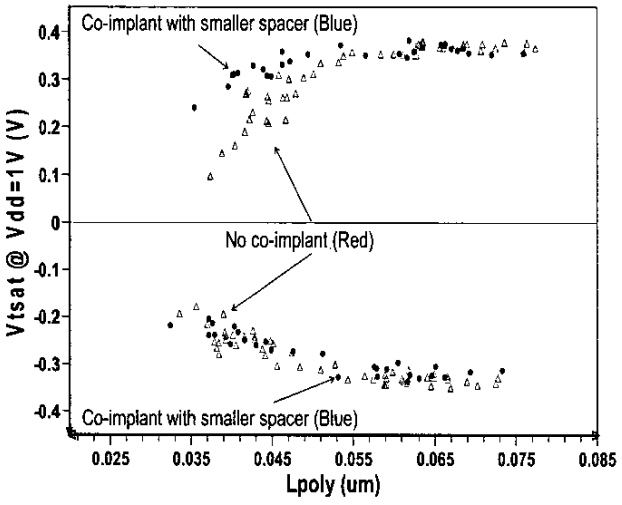

Fig. 5 Co-implants Help Control Vt Roll-off with Slim Spacer

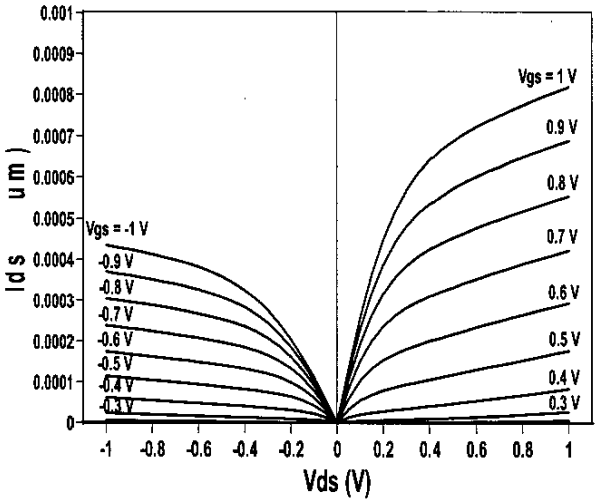

Fig. 6 Output Characteristics for 43 nm Transistors

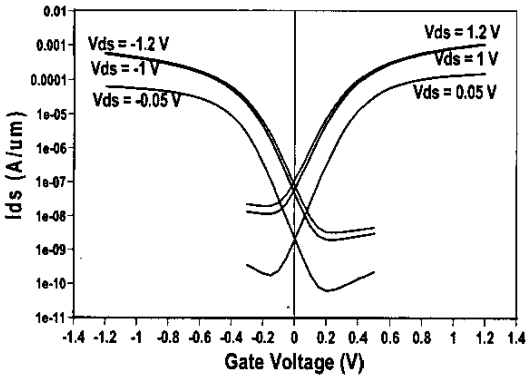

Fig. 7 Sub-threshold Characteristics for 43 nm Transistors

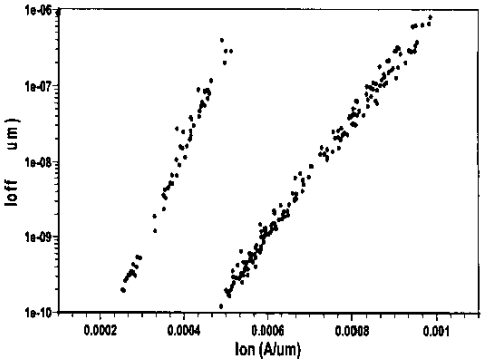

Fig. 8 43 nm Transistors Ion vs. Ioff at |Vdd|=1V

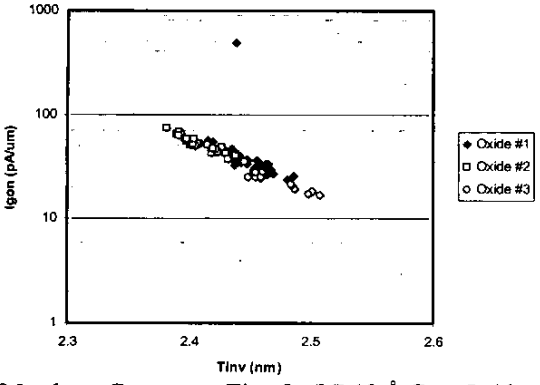

Fig. 9 Leakage Current vs. Tinv for LP 18 Å Gate Oxide

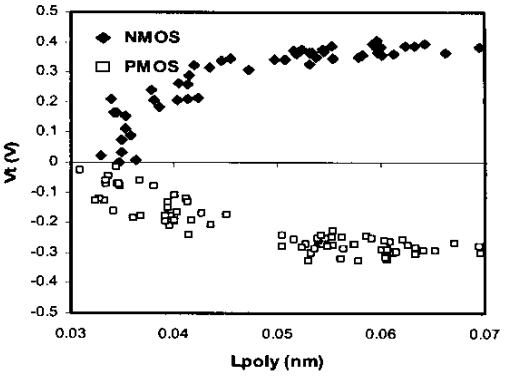

Fig. 10 Vt Roll-off of LP NFET and PFET

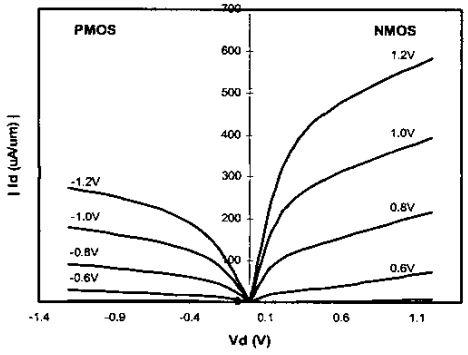

Fig. 11 Output Characteristics for LP 55 nm Transistors

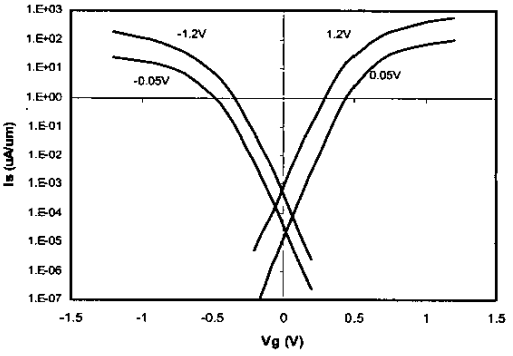

Fig. 12 Sub-threshold Characteristics for LP 55 nm Transistors

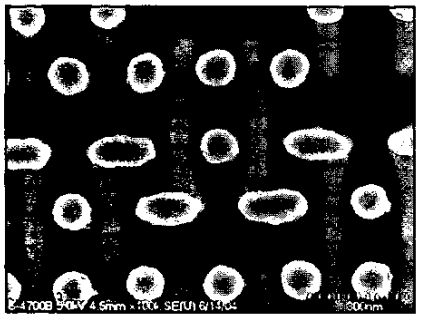

Fig. 13 Top Down SEM of the 0.51μm^2 SRAM cell

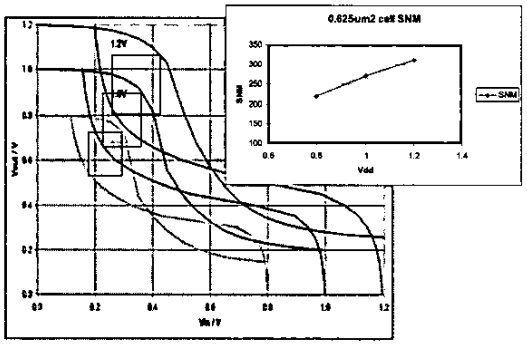

Fig. 14 Butterfly curves of 0.625μm^2 cell