Trimming of Hard-masks by Gaseous Chemical Oxide Removal (COR) for Sub-10nm Gates/Fins, for Gate Length Control and for Embedded Logic

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ABSTRACT

A method for formation and control of silicon gates or fins uses trim of a hard mask by a new gaseous oxide etch. Logic blocks with two separately controlled gate lengths and dielectric thicknesses are embedded on chip.

KEYWORDS

Gate Size Control, Embedded Logic, Scatterometry, Feature Size Reduction, Novel Processes

INTRODUCTION

Channel length control at the 130 nm and below nodes is increasingly difficult. While linewidth variations on single channel length chips are local environment dependent, and very difficult to control even with advanced optical proximity corrections, the problem is even more complex when multiple gate oxide high performance logic devices with different channel lengths need to be controlled to the same precision. (See Figure 1).

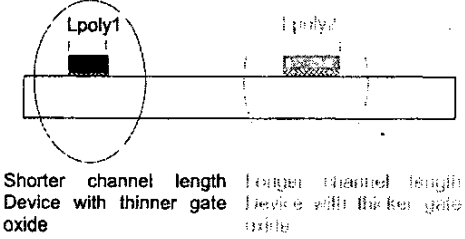

Figure 1. Schematic of chip with multiple gate oxides and channel lengths. L_{poly1} and L_{poly2} need to be controlled independently, to the same tolerance. Both gate hard masks are printed with the same lithographic step but the L_{poly1} hard mask is selectively trimmed to the required size by the COR process without additional OPC or critical masks.

Use of multiple gate oxide devices may arise for a variety of reasons e.g. reuse of already qualified I/P from a previous technology, reduction of standby currents, or need to embed a higher performance block. This paper addresses the challenges of maintaining independent channel length control for two separate devices without the use of additional critical lithographic levels. Furthermore, the new hard mask trim process decouples the absolute size of silicon features from the lithographic size.

COR PROCESS

The Chemical Oxide Removal (COR) process is a new gaseous, plasma-free/damage-free etch using a mixture of HF and NH_3 in a ratio of approximately 2:1. Reaction is carried out at pressures below 15mTorr at 25C to form solid ammonium hexafluorosilicate, followed by evaporation at a temperature over 100C. Oxide (Ozone TEOS) hard mask removal amounts of between about 10-120 Å are controlled by time, pressure, or temperature (Figures 2, 3).

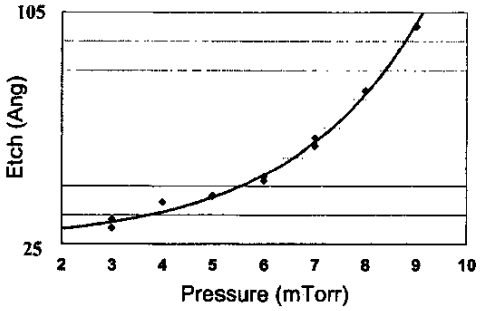

Figure 2. Ozone TEOS etch vs. Pressure for HF:NH_3 ratio of 2.0 and temperature of 25C.

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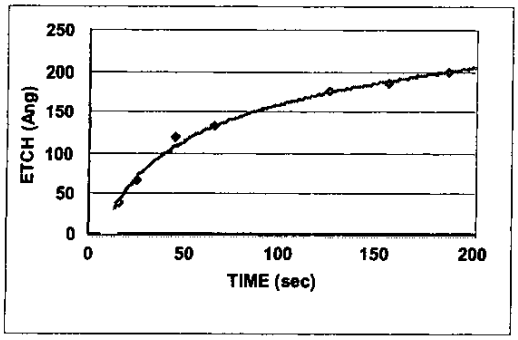

Figure 3 Thermal oxide etch amount vs. time shows a declining rate with time as the solid reaction product begins to self-limit the reaction by impeding reactant diffusion to the underlying oxide. HF:NH_3 ratio of 2.0, 8mT, 23C.

The solid reaction product is semi-permeable toward the reactants but eventually limits reactant diffusion to the underlying oxide as the reaction product layer grows in thickness. This self-limiting reaction contributes properties favorable for many applications including enhanced control. Even un-annealed TEOS can be controllably etched. A typical dilute aqueous HF solution preferentially etches un-annealed TEOS with a TEOS:Thermal oxide selectivity of 8:1; in contrast, the COR process preferentially etches thermal oxide with a TEOS:Thermal oxide selectivity as small as 0.5:1.

PROCESS FOR CONTROL/REDUCTION OF GATE/FIN SIZE

The process for reduction of gate/fin size shown in Figure 4 uses controlled, lateral COR trim of an intermediate ozone TEOS or thermal oxide mask which was produced by RIE of an overlying resist pattern. The mask trim is only lateral because the intermediate TEOS or thermal oxide mask layer was topped with a 45-90 Å COR resistant layer (sputtered Si or LP nitride) prior to patterning.

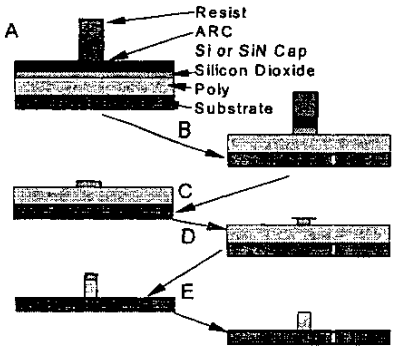

Figure 4. Silicon size is reduced by first patterning a Si or Si_2N_3 topped TEOS layer (A,B,C). COR etch of the topped TEOS is lateral (D). Trimmed TEOS is a mask for Silicon RIE (E).

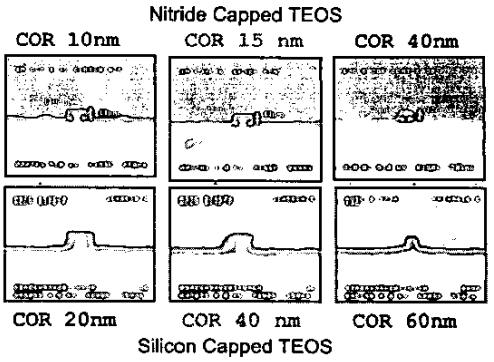

Figure 5. Lateral COR trim of TEOS mask capped by silicon (bottom) or silicon nitride (top).

The oxide features which are laterally trimmed by COR (see Figure 5) are then used to mask the subsequent silicon RIE to produce Fin or gate. Note that the oxide features are trimmed in lateral dimension from two sides. This gives rise to a 1:1 relationship between two times the blanket oxide etch amount (the expected COR trim) and the final electrically measured CD (see Figure 6) when the oxide features are capped by the sputtered Si, COR resistant layer.

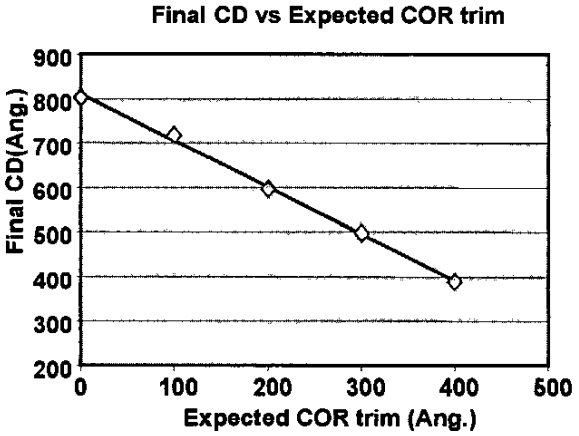

Figure 6. Reduction in the final critical dimension of the silicon feature (Final CD) is linear in the expected COR trim based on a blanket oxide monitor. (Si cap on TEOS mask) The expected COR trim amount is two times the etch of a blanket oxide monitor.

Minimum sizes when coupled with RIE resist trim are independent of use of 248nm or 193nm lithography. Achieved dimensions have progressed from the Si sizes needed for 15nm FinFETs [1] and the 6-60nm polysilicon gate dimensions of reference [2] to the sub-10nm silicon profiles of Figure 7.

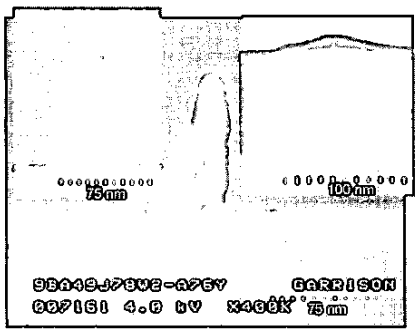

Figure 7. Small silicon structures

In contrast to plasma trims of resist, the plasma-free COR trim has minimal to no bias between nested and isolated features, is independent of local pattern factor and trims of 110nm were achieved with repetition of the COR trim. These properties decouple final feature size from both the lithography and the RIE resist trim/oxide mask open processes. For the first time there is a path whereby the lithography step and the RIE mask open steps can be optimized without regard to the final device size.

EMBEDDED LOGIC BLOCKS

The oxide hard mask can be blocked in certain locations with a non-critical resist mask prior to COR trim (Figure 8). The open regions become smaller L_{poly} (Figure 9), higher performance, independently COR-controlled regions on the same chip. These regions accommodate reuse of already qualified I/P from a previous technology, a need to reduce standby currents, or need to embed a higher performance block. Figure 10 shows higher performance, COR trimmed ring oscillators on 17 Å gate dielectric embedded along with untrimmed, lithography-controlled, ring oscillators on 22 Å dielectric.

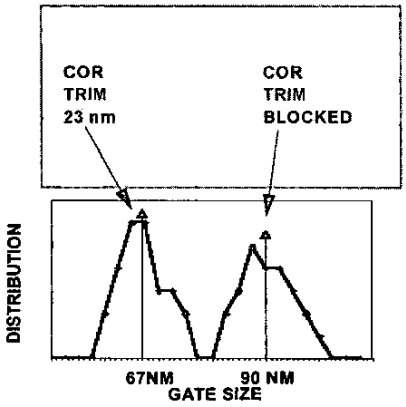

Figure 8. Blocking the COR trim with a resist mask in a portion of the chip produces two gate sizes. The two size distributions are separated by the trim amount. The spread in size distributions arises from a lithographic dose stripe.

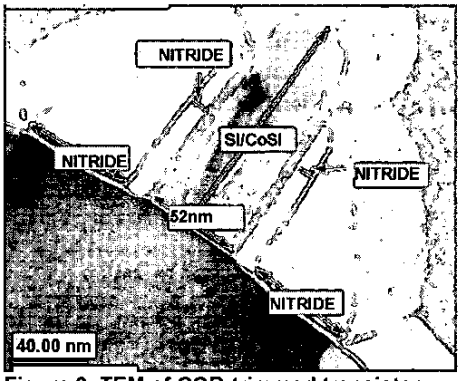

Figure 9. TEM of COR trimmed transistor.

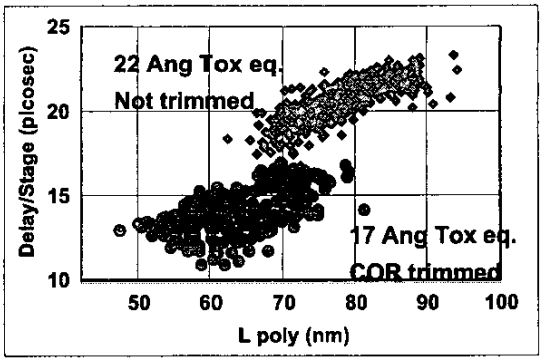

Figure 10. Unloaded inverter ring oscillators at 1.2V. Green diamonds are untrimmed and blue diamonds are trimmed 15nm by COR. The spread in size distributions arises from a lithographic dose stripe.

GATE SIZE CONTROL

Gate size control becomes increasingly important as the absolute size of a transistor decreases. Off current increases exponentially as the gate length is decreased., Precise control of gate lengths enables production of the smallest possible devices for the highest possible performance without exceeding the off current requirements of the chip. Furthermore, when a COR trimmed block of transistors is embedded on a chip, then two transistors of different size and different gate dielectric thickness must both be controlled to optimize overall chip performance. The following section describes wafer to wafer or lot to lot control of the lot average or wafer average transistor size. Two separate control points are needed to meet our goal of independent control of the dimension of both the large L_{poly} and small L_{poly} devices. One control point is provided by RIE resist trim and the second control point is provided by the COR trim of an oxide hard mask. Discussion will focus on control using the new COR trim process.

COR Control of Gate Size with Two Device Lengths Integrated on Chip.

The first control point within the process sequence for gate formation shown in Figure 11 can be exercised by first measuring resist critical dimension (CD). Then the dimensional information can be fed forward to an adjustable RIE resist trim/ARC open step which compensates variations in the size of the large L_{poly} and small L_{poly} devices. When the resist CD of the large L_{poly} device is too large, a large trim can bring the dimension down to the target size. When the resist size is too small, then a smaller than nominal trim can produce a final dimension at the target size. Optimization of the size of the large L_{poly} device occurs without regard to the size of the devices which are eventually to become the small L_{poly} devices. The resist features which mask the TEOS hard mask of the small L_{poly} devices are also changed in size by the process described above, but they are not directly controlled in size. Control of the size of the small L_{poly} devices occurs at the second control point.

The second control point occurs after TEOS RIE and resist ash, and after a non-critical resist mask (not shown) is placed on the large L_{poly} TEOS masks, but prior to COR etch. Dimension of the TEOS mask of the embedded, unmasked, smaller L_{poly} block can be controlled by measuring the hard mask and adjusting the COR trim in a fashion similar to that described above for the resist trim control point. Final gate dimensions can be measured after silicon RIE.

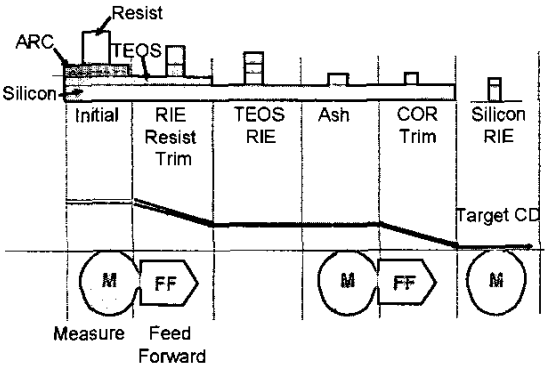

Figure 11. There are two control points in the gate formation process sequence where size or critical dimension (CD) measurements (blue circle) can be fed forward (red arrow) to an adjustable compensating trim. One is located prior to RIE resist trim and the other is located prior to COR trim of the TEOS hard mask. Final CD is measured after silicon RIE.

Demonstration of COR Control

An 8.5nm hard TEOS mask size variation, as measured by CDSEM, was manually fed forward to control a variable, compensating COR trim. Final polysilicon size spreads were reduced to 1nm (Figure 12).

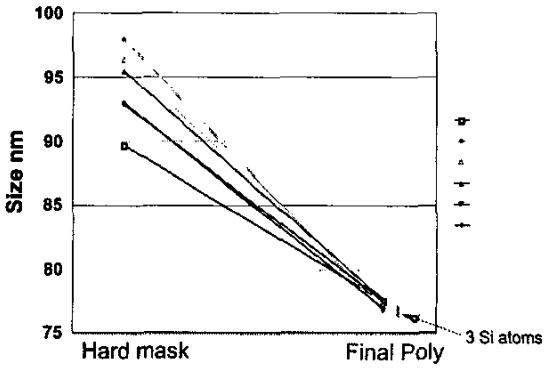

Figure 12. An initial spread in wafer average mask size of 8.5nm was reduced to less than 1nm by an adjustable COR trim.

Scatterometry is a more easily integrated, less costly way to measure hard mask sizes than is a CDSEM. Figure 13 shows a comparison between intra-wafer mask sizes determined by CDSEM and by scatterometry. Measurement correlations similar to Figure 13 have also been obtained for wafer to wafer measurements within a lot of wafers. An adjustable COR trim based on a wafer average mask size measured by scatterometry yielded results similar to Figure 12 but with a spread in final gate size of 1.6nm (3s), as measured by the CDSEM [3].

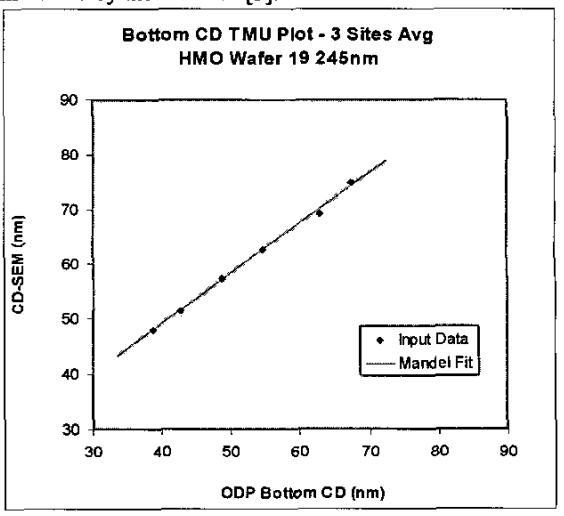

Figure 13. Intra-wafer CD as determined by CD-SEM and scatterometry (ODP). The Total Measurement Uncertainty (TMU), a 3 sigma metric of the scatterometer's measurement uncertainty [4], is 0.7nm. Points are the average of 3 sites. Measured CD's can differ from physical CD's by a constant.

Control Systems and Methods

An integrated tool incorporating COR, RIE and scatterometry is being optimized for automated gate size control for reduction of wafer to wafer and lot to lot size variations.

Both the factory and the integrated RIE/COR/scatterometer tool are equipped with Advanced Process Control (APC) systems, with the on-board tool system interfacing directly with the integrated scatterometer. The APC systems automate the procedures for calculating the size deviation from target and for selecting the process parameters needed for a trim which compensates size variations. When a factory and tool both have APC systems, the control method can operate within the factory, within the tool, or can explore synergies arising from shared control.

There are a number of challenges associated with integration of the tool systems and the factory systems[5]. In addition to the standard RIE tool controller used for process recipes and chamber sequencing, there are recipes which include needed control variables for the on-board tool APC controller, for definition of error handling protocols, alignment recipes to find scatterometer measurement sites, and scatterometer models for interpreting spectra and for generating measurements of the resist mask dimensions, hard mask dimensions, and final gate dimensions. It is also necessary to integrate reporting of measurements, reporting of process conditions selected by the tool controller and communication of error handling and fault detection events with the factory system in addition to recipe integration.

CONCLUSION

Ultra small devices, embedded higher performance logic, and wafer gate length control are enabled by a new method, using a Chemical Oxide Removal (COR) trim of a hard mask. The method decouples final feature size from lithography and from the RIE resist trim/oxide mask open processes. When a chip includes gates of multiple gate lengths and gate dielectric thicknesses, the new method, in concert with RIE resist trim, can provide independent adjustment and control of two separate gate lengths. COR control has achieved final size spreads of 1 to 2 nm using measurements from either the factory CDSEM or from a scatterometer integrated on the process tool.

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