meter CMOS, high-voltage IC's, dielectrically isolated bipolar IC's, and radiation-hardened IC's. Wafer bonding is probably the most versatile SOI technique developed thus far.

*Fujitsu Limited.

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IIA-1 Reduction of Hot-Electron-Generated Substrate Current in Sub-100-nm Channel Length Si MOSFET's—G. G. Shahidi, D. A. Antoniadis, and Henry. I. Smith, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139.

Channel-hot-electron-generated substrate current was measured in MOSFET's with channel lengths down to 0.09 μm, at room temperature and 77 K, and a reduction of the normalized substrate current, I_{SUB}/I_D, was observed for very short channel devices. These devices were fabricated using X-ray lithography, and had a nonuniformly doped channel [1]. The oxide thickness was 4.8 nm. For devices with $L > 0.5$ μm a plot of I_{SUB}/I_D versus $(V_{DS}-V_{DSAT})^{-1}$ is a straight line independent of channel length, as predicted by the lucky electron model [2]. V_{DS} and V_{DSAT} are the drain-to-source and the drain saturation voltages, respectively. This shows that the peak field in the channel, E_m, depends only on $(V_{DS} - V_{DSAT})^{-1}$, and is independent of channel length for long-channel-length devices. As the channel length was reduced below 0.5 μm, the plots of log $(I_{SUB}/I_D$ versus $(V_{DS} - V_{DSAT})^{-1}$ remain a straight line, but become channel length dependent, and shift upward, i.e., I_{SUB}/I_D at a given $(V_{DS} - V_{DSAT})^{-1}$ increases. This suggests that E_m at a given $(V_{DS} - V_{DSAT})^{-1}$, becomes a function of L for $L < 0.5$ μm. We have verified this using the two-dimensional simulator, MINIMOS. As channel length is reduced below 0.15 μm, however, the lines shift down, i.e., I_{SUB}/I_D at a given $(V_{DS} - V_{DSAT})^{-1}$ decreases even though E_m is expected to continue to increase. This new behavior occurs at about the channel length where the effective carrier velocity, calculated from the staturated intrinsic transconductance, exceeds the bulk saturation velocity [1]. We believe that the reduction of I_{SUB} in ultrashort channel MOSFET's is caused by: 1) a reduction of the electron temperature in the channel relative to the steady-state temperature that corresponds to the lateral field, and 2) electron velocity overshoot over a significant part of the channel leading to a reduction in carrier density.

Substrate current was also measured at 77 K. The most interesting phenomenon is a significant reduction in the magnitude of substrate current for short-channel device at 77 K at large V_{DS}. In long-channel devices, $L > 0.5$ μm, both I_D and I_{SUB} increase at 77 K at large V_{DS} from their value at 300 K, but in short-channel devices, $L < 0.5$ μm, I_{SUB} is reduced even though I_D increases. In long-channel devices, plots of log $I_{SUB}/I_D)$ versus $(V_{DS} - V_{DSAT})^{-1}$ at 77 and 300 K have a crossover, as previously reported [3], [4]. For short-channel devices the crossover has shifted to very high V_{DS}, beyond the range of measurement.

We have also used indium as an alternative channel implant. Indium has an atomic weight of 115, and the implant peak can be placed very close to the surface. The profile is skewed toward the bulk, resulting in very light surface concentration. In addition to enhanced low-field mobility, threshold, and transconductance, the increase in I_{SUB}/I_D for $L < 0.5$ μm is not observed for some implant energies. Only the reduction in normalized I_{SUB} for devices with $L < 0.15$ μm is seen.

In conclusion we have shown a reduction in hot-electron-generated substrate current for short-channel MOSFET's at 300 and 77 K. We attribute this to non-local effects caused by the finite energy relaxation time.

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Student paper.

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IIA-2 Subhalf-Micrometer Buried-Channel PFET Design Considerations—E. J. Nowak, A. Bhattacharyya, A. Klett, R. W. Mann, IBM General Technology Division, Essex Junction, VT 05452.

Design considerations for subhalf-micrometer buried-channel PFET's are discussed for 3.3-V technology applications. The device technology employs scaled gate-oxide thickness (14 nm), salicided gate electrode and junctions, and high-temperature glass passivation.

Conventional design approach employs a uniform n-well profile (UNW). Device scaling considerations require increased doping level for UNW to contol short-channel effects such as FET threshold and punchthrough voltage reduction. Increased junction capacitance, wider FET threshold-voltage tolerance, and decreased low-field hole mobility are consequences of the increased UNW doping level. Reduction of these effects is accomplished with a nonuniform n-well profile, referred to as a tailored n-well (TNW). Other important factors in FET characteristics are gate sidewall spacer thickness and silicide–silicon interface doping. These effects are explored and analyzed to provide an optimal PFET design.

Tailored n-well profiles are achieved with deep phosphorus implants (DPI). Modeled profiles compare well with experimental results from devices fabricated with DPI in the range of 150 to 200 keV. The TNW devices equal or exceed the short-channel characteristics of the UNW devices with junction capacitance reduced by 40 percent. Improvements in linear transconductance and threshold-voltage tolerance are also achieved.

Additional improvements in PFET performance are available by reduction of parasitic overlap capacitance (C_o/l) and device series resistance (R_s). Overlap capacitance decreases with increasing spacer thickness with a slope nearly equal to the gate-oxide capacitance while the R_s increases. The PFET R_s is further affected by the boron concentration in the silicon at the silicide–silicon interface. Thermal conditions used in the glass passivation are explored with respect to series resistance through this mechanism.

PFET characteristics at 350-nm channel lengths are obtained with saturated transconductance of 88 mS/mm, 0.6 fF/μm^2 junction capacitance, and good subthreshold characteristics.

IIA-3 High-Performance Submicrometer Channel MOSFET's for Analog Applications—Merit Y. Hung and Dimitri A. Antoniadis, Massachusetts Institute of Technology, Cambridge, MA 021239.

Thus use of MOSFET's in analog circuits is gaining increasing interest due to their low power, high packing density, and ease of