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A High Performance 0.13µm SOI CMOS Technology with Cu Interconnects and Low-k BEOL Dielectric

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Introduction

This paper describes a 1.2V high performance 0.13 µm generation SOI technology. Aggressive groundrules and a tungsten damascene local interconnect render the densest 6T SRAM reported to date with a cell area of 2.16 μm^2. This is accomplished with 248nm lithography, using optical proximity correction and resolution enhancement techniques on all critical levels. Interconnect performance requirements are achieved by using up to 8 levels of Cu wiring and an advanced low-k interlevel dielectric.

Process Integration

The technology presented in this paper is a 1.2V high performance SOI CMOS logic process that includes dual gate oxide thicknesses for support of 1.5/1.8V I/O circuits. It incorporates a 6T SRAM cell with an area of 2.16μm^2, requiring three levels of metal. This compares to a 4.23 μm^2 SRAM cell size for the previous technology node[1]. Key groundrules are listed in Table 1. A top down SEM image of the SRAM cell is shown in figure 1. Functionality of the SRAM down to a power supply of 0.8V is demonstrated in figure 2. Extensive calibrated aerial image modeling was used to determine the optimal proximity corrections for all critical levels. As an example, the resulting mask data for the local interconnect level is shown in figure 3. Figures 4 and 5 show top down SEM images of the local interconnect level in the SRAM cell with and without the OPC optimization.

Transistors and Reliability

SOI permits device design down to very small gate lengths with excellent short channel control [2]. As shown in figure 6, the short channel effects in this technology are well controlled down to design lengths of 85 nm. NMOS and PMOS drive currents at 100 nA/µm off current and 1.2V VDD are 830 µA/µm for NFET and 450 µA/µm for PFET, with threshold voltages of 170 mV for both NFET and PFET. The Ion-Ioff characteristics are shown in figure 7. Multiple threshold voltage devices are offered to support a range of applications, as outlined in table 2. The standard 1.2V device has the highest performance reported to date; offering a sub-17 psec delay for a 3-way NAND. In addition, lower and higher Vth devices, for operation at 1.2V, are provided to maximize product performance while meeting leakage, power and reliability constraints [3]. The lower Vt device, used in circuits that are most sensitive to the Vt/Vdd ratio and in critical paths, offers 18% higher performance. The higher Vt device, used in dynamic nodes and in large SRAM arrays to minimize Iddq, offers a 10x reduction in Ioff.

The gate leakage current in the 2.6 nm gate oxide is supressed by optimizing the nitrogen content in the dielectric. A 3-5X reduction in gate current is achieved with this gate oxide over conventional oxynitrides of the same equivalent thickness, figure 8. As shown in figure 9, the dielectric time to fail of the 2.6 nm gate oxide meets the requirements for 1.2V operation including tolerances. Excellent hot carrier reliability is also demonstrated in this technology, figures 10 and 11.

Interconnect Performance

Interconnect performance was assessed quantitatively by a model that calculates RC delay of an equal weighting of local, mixed and global nets, and takes into account the wireability of the chip and resulting die size. The resulting interconnect performance metric is show in figure 12 as a function of technology generation for IBM's high performance logic technologies. The change in slope after 0.25µm technology was due to the introduction of Cu interconnects. In order to maintain the performance scaling into the 0.13um generation an advanced low-k dielectric and 8 levels of Cu wiring is required. The Cu metalization is produced by a dual damascene process at all levels, eliminating the need for an embedded etch or polish stop in the low-k material between line levels and the previous via level. In addition, hierarchical wiring with 4 different metal pitches and layer thicknesses is provided for optimal performance of global wiring, power distribution and density. This hierachical wiring scheme accounts for ~5% performance increase over a technology with only 2 different pitches in the same materials system.

Conclusion

The fabrication of a high performance 0.13um SOI logic technology with copper BEOL and advanced low-k dielectric is demonstrated using 248nm lithography for all critical levels. The interconnect performance requirements are met by using a 8 level copper BEOL with an advanced low-k dielectric. This technology supports an SRAM cell size of 2.16 μm^2, the smallest reported to date.

Acknowledgements

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References

1. E. Leobandung et al., IEDM Tech. Dig., pp. 697, (1999).
2. I. Yang et al., IEDM Tech. Dig., pp. 148 , (1999).
3. K. Bernstein et al. Submitted VLSI Tech Symp (1999).

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Level	Pitch (µm)
Active	0.35
Gate	0.325
Loc. IC	0.325
Contact	0.35
M1	0.35

Table 1: Key design rules

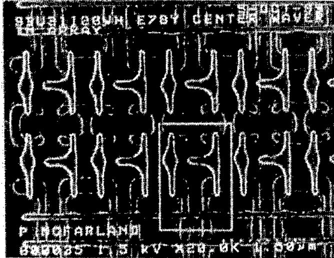

Fig. 1: SEM Image of 2.16 µm^2 SRAM cell

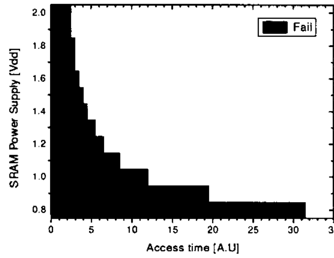

Fig. 2: SRAM functionality

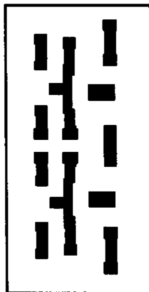

Fig. 3: Design and OPC corrected mask data for local interconnect pattern

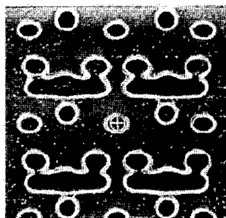

Fig. 4: Non OPC optimized local interconnect pattern in SRAM cell

Device Offering	Vt [mV]	Ioff [nA/µm]	3-Way Nand delay [psec]	Application
Low-Vt	170	100	14	Vt/Vdd sensitive circuits and critical paths
Standard Vt	250	10	16.8	Logic
High-Vt	330	1	22.2	SRAM for Iddq and dynamic nodes

Table 2: Device offerings

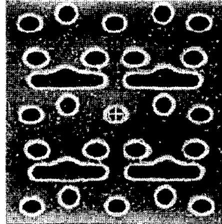

Fig. 5: OPC optimized local interconnect pattern in SRAM cell

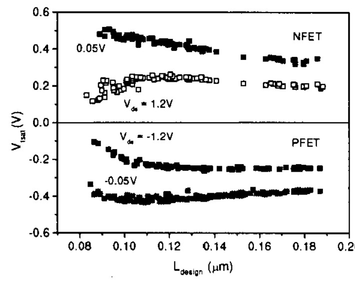

Fig. 6: Threshold voltage roll-off

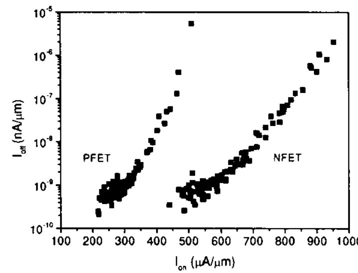

Fig. 7: Ion-Ioff characteristics

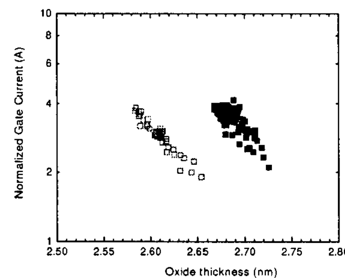

Fig. 8: Gate tunneling current as a function of gate oxide thickness

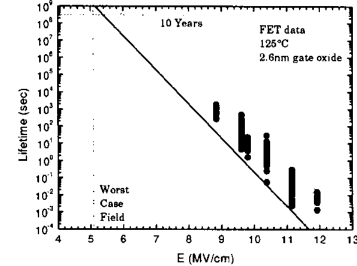

Fig. 9: Dielectric reliability for 2.6 nm oxide

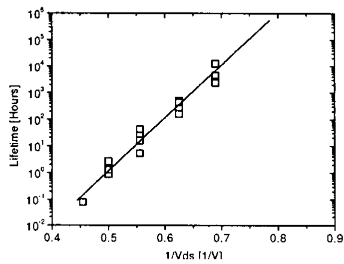

Fig. 10: Hot electron lifetime for NFETs

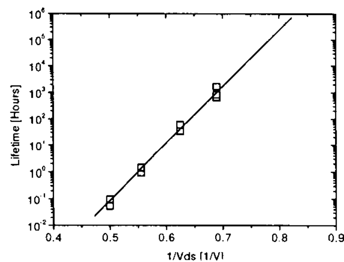

Fig. 11: Hot electron lifetime for PFETs

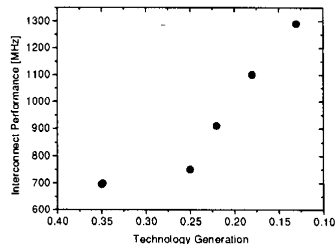

Figure 12: Interconnect Performance as a function of technology generation

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