65nm CMOS Technology for low power applications

A. Steegen, R. Mo, R. Mann M.-C. Sun[3], M. Eller[2], G. Leake , D. Vietzke[2], A. Tilke[2], F. Guarin, A. Fischer[2], T. Pompl[2], G. Massey, A. Vayshenker, W.L. Tan[1], A. Ebert, W. Lin[1], W. Gao[1], J. Lian[2], J.-P. Kim[3], P. Wrschka, J.-H. Yang[3], A. Ajmera, R. Knoefler[2], Y.-W. Teh[1], F. Jamin, J.E. Park[3], K. Hooper, C. Griffin, P. Nguyen, V. Klee[2], V. Ku, C. Baiocco, G. Johnson, L. Tai, J. Benedict, S. Scheer, H. Zhuang[2], V. Ramanchandran, G. Matusiewicz, Y.-H. Lin, Y.K. Siew[1], F. Zhang[1], L.S. Leong[1], S.L. Liew[1], K.C park[3], K.-W. Lee[3], D.H. Hong[3], S.-M. Choi[3], E. Kaltalioglu[2], S.O. Kim[2], M. Naujok[2], M. Sherony, A. Cowley, A. Thomas, J. Sudijohno[1], T. Schiml[2], J.-H. Ku[3], I. Yang

IBM Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY 12533
[1]Chartered Semiconductor Manufacturing, [2]Infineon Technologies AG, [3]Samsung Electronics Co., Ltd

Abstract

This paper presents a 65nm low power technology offering a dual gate oxide process, multiple Vt devices at a nominal operating voltage of 1.2V, a nine level hierarchical Cu interconnect back-end of line process with low k dielectrics and 0.676µm^2 and 0.54µm^2 SRAM cells, optimized for performance and density, respectively. The key focus of this technology has been low cost, process simplicity and power reduction. A gate dielectric with an nfet leakage current as low as 15pA/µm and with exceptional reliability characteristics has been demonstrated. Moreover, competitive drive current has been achieved, 725/343uA/um at an off current of 7nA/um for n/pfets at nominal voltage. A pfet performance enhancement of an additional 13% at 7nA/um off current was achieved by using mobility enhancement techniques without adding process complexity. An optimized NiSi process and high angle, low dose halo implants contribute to the reduced junction leakage and GIDL current.

Introduction

The most urgent demands for low power electronics originate from the stringent requirements for small size and weight, low cost, long operating life and reliability of battery operated applications. This paper presents a 65nm low power technology offering a dual gate oxide process and multiple Vt devices at a nominal operating voltage of 1.2V. The use of a third gate oxide is optional. A leading edge 193nm lithography process used on critical levels enables aggressive 0.7x scaling and direct design migration from the previous technology node without design rule restrictions and supports dense SRAM cells with an area size down to 0.49um^2. Key elements of this technology are low cost, process simplicity and power reduction. The gate leakage current has been reduced to 15pA/um, twice as low as earlier reported [1] with excellent reliability characteristics. A competitive drive current has been achieved, 725/343uA/um at an off current of 7nA/um for n/pfets at 1.2V operation voltage [2,3]. Moreover, a pfet performance enhancement of an additional 13% at 7nA/um off current was achieved by using mobility enhancement techniques without adding process complexity. An optimized NiSi process and high angle, low dose halo implants contribute to the reduced junction leakage and GIDL current. This technology utilizes an advanced low k BEOL integration of nine levels with copper for both wirebond and Flip Chip package offerings.

Key Process Features and Device Characteristics

The 65nm low power technology is a CMOS 65nm generation application-specific integrated circuit (ASIC) and foundry technology developed for static random access memory (SRAM), logic, mixed signal, mixed voltage I/O applications and is a platform for embedded DRAM applications. The key technology pitches are listed in Table 1.

65nm Low Power Technology	*Pitch (line/space) [µm]*
N+/P+	*0.30*
Active area	*0.20 (0.10/0.10)*
Gate (minimum)	*0.22 (0.06/0.16)*
Gate (contacted)	*0.26 (0.06/0.20)*
Contact	*0.225 (0.09/0.135)*
M1	*0.18 (0.09/0.09)*
Mx	*0.20 (0.10/0.10)*

Table 1: Key 65nm low power technology pitches.

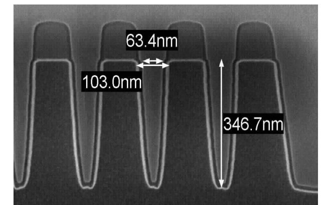

Fig.1: Void free 350nm deep shallow trench isolation using oxide based one step fill process with in situ NF3 etch back.

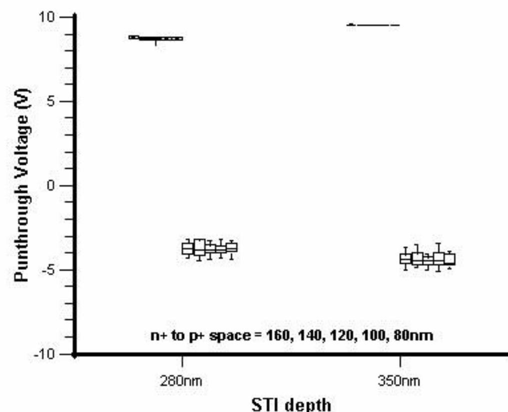

Fig 2: Break down voltage for 350nm and 280nm isolation process for N+/P+ spacings from 160nm down to 80nm.

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This technology features a void free 350nm deep shallow trench isolation process (Fig.1) with excellent isolation characteristics down to 0.080µm N+/P+ spacing (Fig.2). A one step oxide based fill process with NF_3 etch back is used to fill the trenches shown in Fig.1. Recent results demonstrate equivalent break down voltages for a 280nm deep trench (Fig.2), simplifying the oxide fill scheme even further. The poly-silicon gate length is 55nm for both nfet and pfet. Fig.3 shows a cross sectional image of the transistor. This technology offers three oxide options with physical thicknesses of 20A, 28A and 52A at 1.2V, 1.8V and 2.5V operation voltages, respectively. Fig.4 shows a TEM image of the high performance gate oxide.

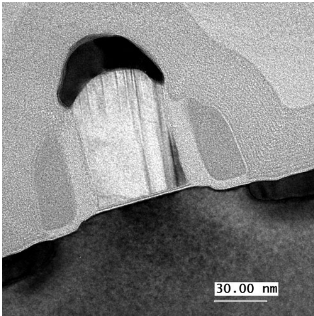

Fig 3 : TEM image of 55nm long gate stack.

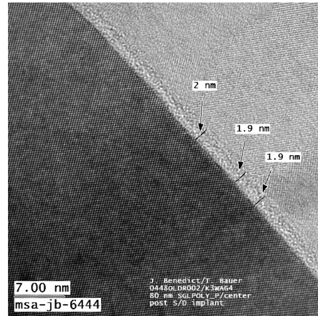

Fig.4: TEM image of high performance gate oxide.

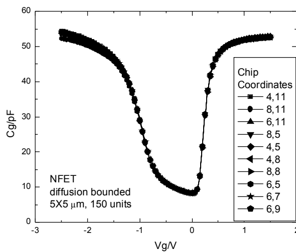

Fig.5a: Thin oxide nfet CV.

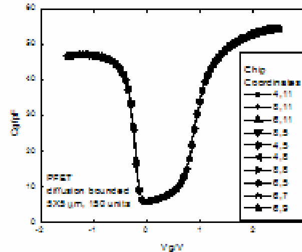

Fig.5b: Thin oxide pfet CV.

CV characteristics are shown in Fig.5a and 5b for nfet and pfet, respectively. The high performance oxide gate leakage current as a function of the oxide thickness under inversion for various process conditions is illustrated in Fig.6 (nfet).

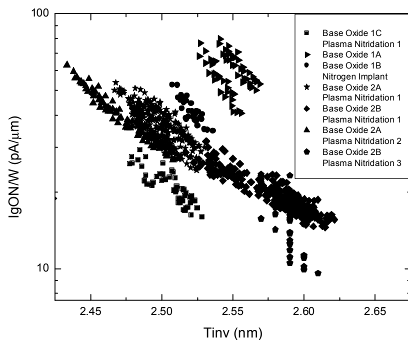

Fig.6: Gate leakage current as function of nfet inversion current for different types of gate oxide.

The process development effort concentrated on both the base oxide and nitridation processes. Both the nitrogen dose and the base oxide growth mechanism contribute to the superior leakage reduction of the preferred gate oxide (oxide 1C with plasma nitridation 1) with respect to other techniques as indicated in Fig.6. The low nitrogen concentration at the silicon interface as measured with angled resolved X-ray photo-electron spectroscopy (Fig.7) helps us maintain nearly SiO_2 mobility, excellent hot carrier performance and an NBTI shift of as low as 25mV (Fig.8).

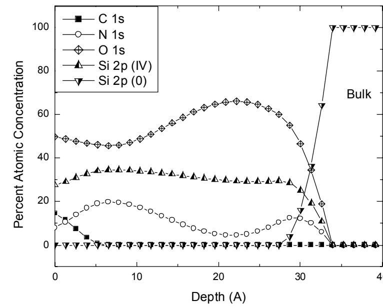

Fig.7: XPS profiles for O and N concentration in the preferred gate oxide.

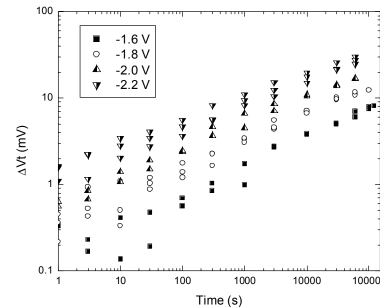

Fig 8: NBTI Vt shift as function of time for different gate voltages.

Base oxide improvements as well as a post nitridation recovery anneal significantly improve the TDDB characteristics of the 20A gate oxide for nfet and pfet as indicated in Fig.9a and 9b respectively.

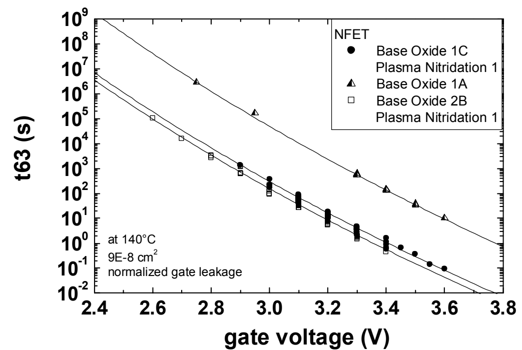

Fig 9a: nfet TDDB: t63 as function of gate voltage for different types of gate oxides.

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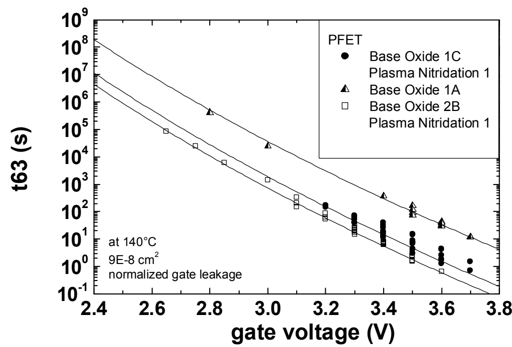

Fig.9b: pfet TDDB: t63 as function of gate voltage for different types of gate oxide.

A competitive current drive of 725/343µA/µm at an off current of 7nA/um and of 600/275µA/µm at an off current of 0.3nA/um has been demonstrated (Fig.10a, 10b) [2,3].

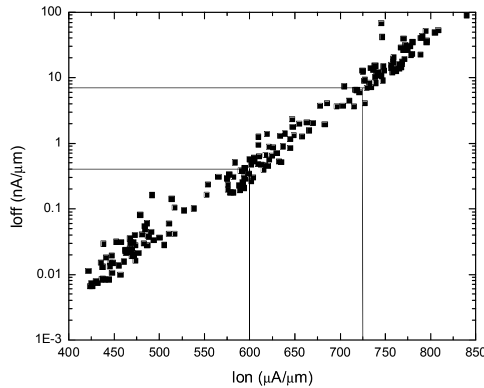

Fig.10a: Nfet Ion/Ioff performance.

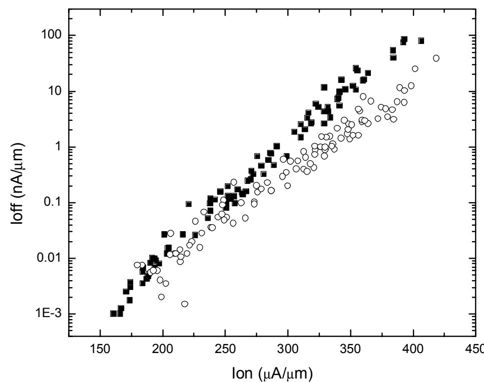

Fig.10b: Pfet Ion/Ioff performance, after device optimization 13% performance enhancement has been achieved.

A pfet performance enhancement of an additional 13% at 7nA/um off current was achieved by using mobility enhancement techniques without adding process complexity (Fig.10b). The low (LVt), regular (RVt) and high (HVt) Vt devices with a nominal gate length of 55nm show good Vt-roll-off down to 45nm (Fig.11).

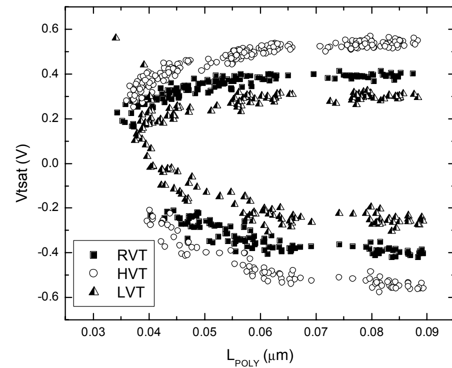

Fig.11: Nfet/Pfet Vt as a function of gate length for different device offerings.

An ultra low nfet gate leakage current of 15pA/um has been achieved (Fig.6). Both nfet and pfet achieve GIDL currents less than 10pA/µm.

This is the first low power generation to introduce NiSi. The main benefits of NiSi compared to $CoSi_2$ are reduced resistance of narrow lines, the ability to move to shallower junctions combined with reduced junction leakage due to less Si consumption and the lower resistivity of NiSi and improved device performance as a result of the lower silicidation temperature. Fig.12a and 12b show the the N+ poly-silicon and diffusion resistance, respectively, as function of the line width.

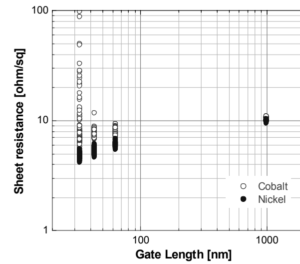

Fig.12a: n+ Poly-silicon resistance as function of poly line width for NiSi and $CoSi_2$.

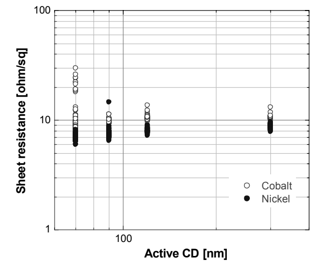

Fig.12b: n+ diffusion region resistance as function of diffusion line width for NiSi and $CoSi_2$.

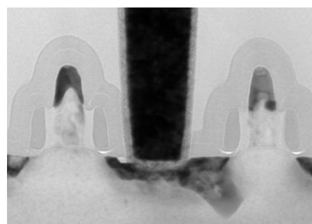

Fig.13a: Non-optimized Ni silicide TEM image (process A) showing enhanced Ni diffusion and the presence of $NiSi_2$.

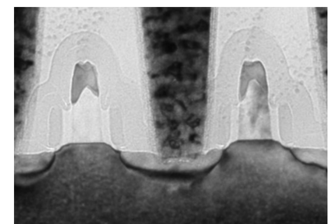

Fig.13b: Optimized Ni silicide TEM image (process B) showing a smooth silicide to Si interface.

At gate lengths below 35nm, the $CoSi_2$ sheet resistance increases drastically compared to NiSi. Optimization of the NiSi process can overcome disadvantages such as a more complex phase formation, enhanced Ni diffusion in silicon, and low thermal stability resulting in the formation of $NiSi_2$. An optimized NiSi process (process B) results in a

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significantly smoother Ni/Si interface (Fig.13), less fallout in leakage current (Fig.14) and the retardation of $NiSi_2$.

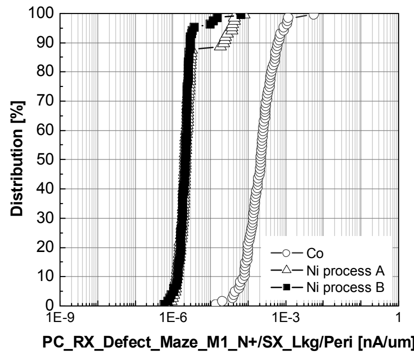

Fig.14: N+ junction leakage for $CoSi_2$ and NiSi.

The benefit in leakage current of this NiSi process is even more pronounced on a specially designed silicide 'pipe' monitor as illustrated in Fig.15a and 15b for P+ and N+ junctions, respectively.

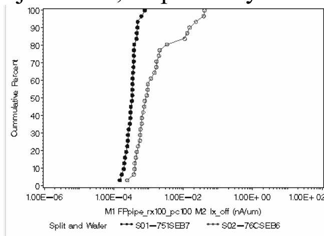

Fig.15a: P+ junction leakage measured on a 'silicide pipe monitor' for a non-optimized (open symbol) and an optimized (solid symbol) NiSi process.

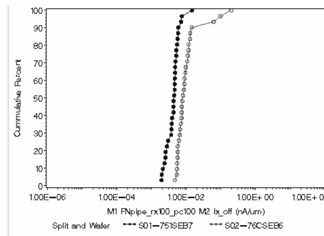

Fig.15b: N+ junction leakage measured on a 'silicide pipe monitor' for a non-optimized (open symbol) and an optimized (solid symbol) NiSi process.

The middle of the line contact module has been altered to avoid high thermal process steps.

SRAM Design

A range of SRAM cell sizes from $0.49\mu m^2$ to $0.68\mu m^2$ are provided for the bulk Si 65nm technology generation. Each is optimized for density, performance or low power. All cell options are split word line designs and use the rectangular contact to achieve the cross coupling. The cells are M2 BL designs but are compatible with M3 BL option. A subset of the critical SRAM bit cell specs are shown in Table 2.

Table 2: Critical SRAM bit cell specs.

Cell Dimensions	*Read current*	*Standby current*	*M2 BL cap*
0.5um x 1.08um	*21 uA*	*<10pA*	*0.21 fF/cell*
0.52um x 1.3um	*33 uA*	*<30pA*	*0.24 fF/cell*

The increase in noise sources, most notably Vt sigma, associated with scaling to 65nm dimensions has demanded extensive optimization of the SRAM cell device dimensions and threshold voltages to adjust the cells for both stability and write margin. The butterfly curves for the $0.54um^2$ low power cell (Fig.16) show > 150mV of SNM down to 0.85V.

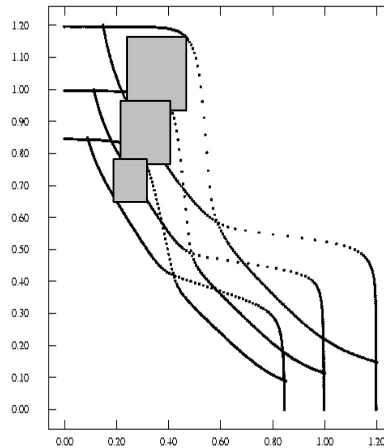

Fig.16: Butterfly curve of $0.54\mu m^2$ cell.

Fig.17 shows a top down SEM of the standard and shared contact configuration used in this cell.

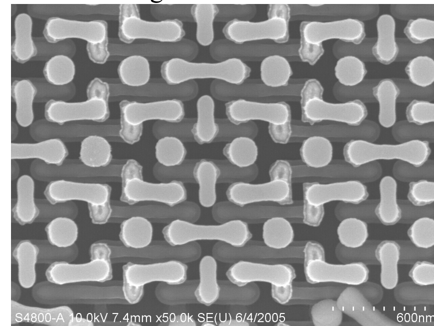

Fig.17: SEM image of the dense cell.

Conclusion

The 65nm low power technology is a conventional gate stack architecture where process simplicity, low cost, high density, high reliability and reduced power consumption are the key focal points. Optimization of the base oxide and nitridation process and the implementation of NiSi improved the leakage current drastically without suffering any performance loss. Both high density and high performance SRAM cells have been successfully fabricated utilizing all of the 65nm features presented in this paper. This leading edge low power technology has already been implemented in early customer products and is on track for high volume manufacturing ramp at the end of 2005.

Acknowledgements

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