Fluctuation Limits & Scaling Opportunities for CMOS SRAM Cells

Azeez Bhavnagarwala, Stephen Kosonocky, Carl Radens†, Kevin Stawiasz, Randy Mann†, Qiuyi Ye†, Ken Chin

IBM T.J. Watson Research Center, Yorktown Heights, NY 10598, †IBM Systems & Technology Group, Hopewell Junction, NY 12533, email: azeezb@watson.ibm.com Tel: (914)945-3869

Abstract

Fundamental limitations on scaling CMOS SRAM cell transistor dimensions and operating voltages are demonstrated by measuring the local stochastic distributions of Read, Write and Retention DC margins of 65nm PDSOI CMOS SRAM cells. DC measurements show, for the first time, the write operation to be more fluctuation limited. Measurements also reveal fundamental insights into terminal voltage dependencies of the fluctuations of cell storage node voltages - observations that are engaged to increase cell immunity to fluctuations by *several* orders of magnitude by biasing the cell terminal voltages appropriately.

Introduction

Previous work on random threshold voltage variations between neighboring, small geometry SRAM cell transistors due to dopant fluctuations [1-4], line edge roughness [5] and poly gate grain size variations [6] have been shown to limit the DC Read stability of SRAMs [7-10]. The impact of VT fluctuations on SRAM cell DC *write margins* is reported in this work, for the first time, and is shown to be the more limiting case. Systematic variations of critical dimension across chip, wafer and lot modulate the local variations by degrading the short channel behavior [11-12] of cell transistors, skewing the cell transistor VT distributions to take on a *voltage dependent and asymmetric form*. Measurements demonstrate the *exponential operating voltage sensitivities* of SRAM failure statistics– opening opportunities to significantly improve SRAM yield by biasing cell virtual ground and the BL precharge levels optimally.

Binary Signal Quantization in SRAM

The SRAM cell operates as a bistable circuit with two distinct stable states during Read and Retention periods (Fig. 1). This mode of circuit operation translates into a requirement of *3 distinct roots* of the Static voltage characteristics of cell storage nodes [13-14]. During a Write operation (Fig. 2), a low BL voltage pulls down the voltage characteristic of the cell node on the same side permitting only *one root* – corresponding to the intended data on the BL. The Write Noise Margin (WNM) equals the smaller of the 2 squares that can fit between the cell static characteristics during a Write operation (Fig 3). Inability to maintain 3 distinct roots during a Read or inability to limit to only 1 root during a Write leads to DC Failure (Fig. 4).

Measurements

A. Stochastic Distribution Measurements: The test structure (Fig. 5) consists of 512 identical cells per macro with the cell storage nodes wired out through a hierarchy of addressable, wide, high-VT, thick oxide CMOS pass gates – that are driven by separate power supplies to suppress leakage from unselected pass-gates to the measured cell node. Figs 6-8 show distributions of static voltage characteristics for Read, Write and Retention operations from 512 'A' cells. The WNM, SNM and Retention Noise Margin (RetNM) distributions in Fig. 8b enable DC fail statistics to be calculated for any array that uses the same cell (Fig 9). Fluctuations in the Read0 and Write0 voltages (defined in Fig 1b, 3) on the right and left sides of the cells are plotted in Fig 10 with their correlation coefficients and demonstrate that the distributions observed in Figs. 6-8 are overwhelmingly random. Fig 11 shows distributions of Read0 and Write0 voltages from 4 different sites and demonstrate the reproducibility of the measured stochastic distributions. The mean and sigma values of SNM and WNM are applied to an error function as shown in Fig 9 to predict the R/W fail count from a sample of 1024 cells. The comparison in Fig 12 demonstrates excellent agreement. The accuracy is limited by sample size and marginal asymmetry in measured distributions.

B. Fluctuation limited Writes: The pull-up PFET in the CMOS SRAM cell primarily serves to compensate charge leaking away from the cell node holding a '1' and is typically sized with minimum width to enable higher density. The Write0 voltage fluctuates due to a voltage divider between the BL at '0' and cell VDD, through the on access NFET and the on pull-up PFET. These are typically the two smallest transistors in the cell resulting in a Write0 fluctuation variance that is over twice the variance of the Read0 fluctuation. A larger variability in the Write0 node directly translates into a larger WNM sigma making a typical cell more write limited by random fluctuations.

C. Fluctuation dependencies on operating voltages: The mean values of measured Vread0, Vtrip, and Vread1 with their 1 sigma deviations are plotted in Fig. 13. Increasing overlap of the Trip and Read0 voltages degrade SNM at lower voltages. Vwrite0 and Vtrip in Fig 14 show (Vwrite0–Vtrip) increasing at lower voltages making it harder for the cell to write – the assistance from cell feedback notwithstanding. Fig 15 shows that cells become significantly more write fluctuation limited at lower voltages. Figure 16 demonstrates the very high sensitivity of fail count to operating voltage – which can be used to advantage, instead, by biasing cell terminal voltages optimally.

D. Fluctuation improvements with BL and VGND bias: Lowering the BL voltage VBL (Fig17) during a Read access shifts the Read0 distribution to the left (Fig 18) without affecting the Trip voltage distributions (Fig 19) improving Read Margins and Read sigma (Fig 20). For VBL drops that exceed VT below VDD, the cell node storing a '1' degrades variance of Vread1, raising Vread0 and it's variance, and increasing overlap of the Vread0 and Vtrip distributions. Thus BL precharge to VDD-VT is the optimal BL voltage for maximum Read margin. Raising VGND during a write access, using a '*Write Assist*' circuit scheme, raises Vtrip and

0-7803-9269-8/05/$20.00 (c) 2005 IEEE

lowers Vwrite0 distributions (Fig 21-24) making it easier for the BL at ground to pull the cell node lower with more margin below the Trip voltage.

References:

[1] D. Burnett, et al, "*Implications of Fundamental Threshold Voltage Variations for High-Density SRAM and Logic Circuits"* Symp. VLSI Tech., June 1994, pp. 15–16
[2] K. Itoh, "*Low Power Memory Design*," Tutorial slides, 1997 ISLPED
[3] D. Frank et al, *"Monte Carlo Modeling of Threshold Variation due to Dopant Fluctuations",* Symp. VLSI Tech, 1999, pp. 169-170, Jun 1999.
[4] P. A. Stolk et al, "*CMOS device optimization for mixed-signal technologies*", IEDM Tech. Dig., pp. 215-218, Dec 2001.
[5] T. Linton et al, "*Determination of the line edge roughness specification for 34 nm devices*", IEDM Tech. Dig., pp. 303 - 306, December 2002.
[6] Shuji Ikeda, "*Technology for High-Density and High-Performance SRAM*", Chap. 5, Ph.D. Dissertation, Tokyo Inst. of Tech., Oct 2003.
[7] A. Bhavnagarwala et al, "*Impact of Intrinsic Fluctuations on CMOS SRAM Cell Stability*", IEEE JSSC, Vol 36, No. 4, pp. 658-665, Apr 01.
[8] K. Takeuchi et al, "*A Study of the threshold voltage variation for ultra-small bulk and SOI CMOS*" IEEE TED. Vol. 48, No. 9, Sep 2001, pp. 1995-2001.
[9] K. Noda, "*SRAM Technology*", 2001 IEDM Short Course.
[10] B. Cheng et al, "*The impact of random doping effects on CMOS SRAM Cell"*Proc. 30th ESSCIRC, pp. 219 - 222, Sept. 2004.
[11] V. De, et al, "*Random MOSFET Parameter Fluctuation Limits to Gigascale Integration*" *Proc*. Symp. VLSI Tech., pp. 198-199, June 1996.
[12] J. Meindl et al. "*The impact of stochastic dopant and interconnect distributions on Gigascale integration*", ISSCC Dig. Feb. 1997
[13] E. Seevinck et al, "*Static-noise margin analysis of MOS SRAM cells*" *IEEE JSSC*, Vol. SC-22, No. 5, Oct 1987, pp. 748-754
[14] J. Lohstroh et al, "*Worst-case static noise margin criteria for logic circuits and their mathematical equivalence*" IEEE JSSC, Vol. SC-18, No. 6, Dec 1983, pp. 803-806

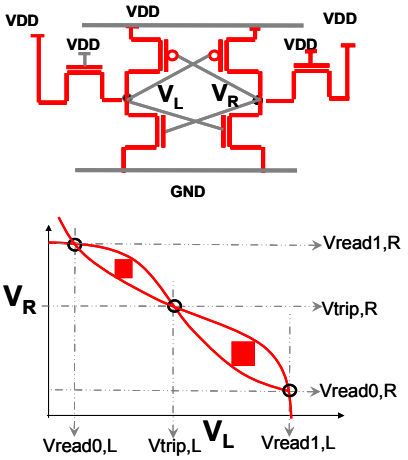

Fig 1a (at left): Schematic of a conventional CMOS SRAM cell during a Read operation.

Fig 1b (at left): Static voltage characteristics of a conv. cell during a read operation. *Three roots (black circles) enable bistable circuit operation.* Smaller of 2 solid squares equals Static Noise Margin.

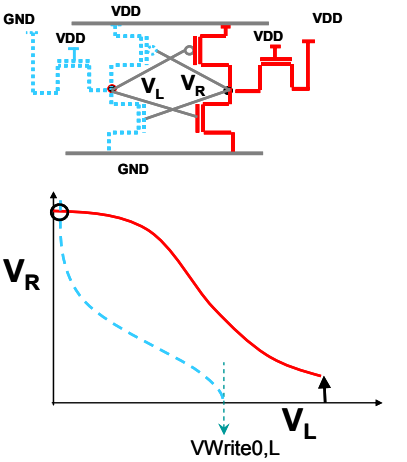

Fig. 2a (at left): Schematic of an SRAM cell during a Write operation.

Fig. 2b (at left): Static voltage characteristics of a conv. Cell during a write operation. The BL at '0' skews the (dotted) voltage characteristic to *permit only one root (black circle),* corresponding to the data on the BL.

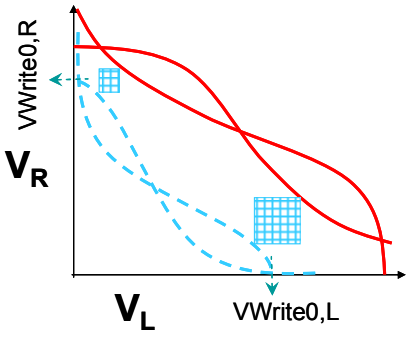

Fig. 3 (at left): Write Noise Margin (WNM) equals the smaller of the 2 smallest squares (check fills) that can be nested between the Write0 (dotted) and Write1 (solid) static characteristics.

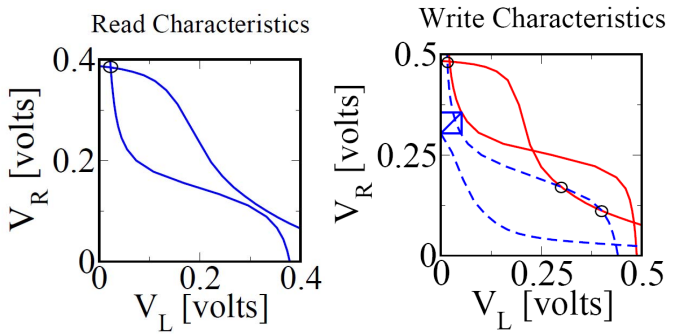

Fig 4 Examples of a measured cell failing a Read (above left) and a Write (above right) operation. The cell failing read cannot operate as a Bistable circuit and the cell failing write cannot operate in Monostable mode.

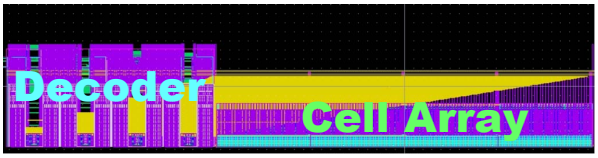

Fig. 5 (above): Test structure to characterize SRAM fluctuations. Cell storage nodes are wired through a hierarchical CMOS pass-gate network to enable characterizing an array of single cells for the purpose of measuring stochastic distributions of cell storage node voltages.

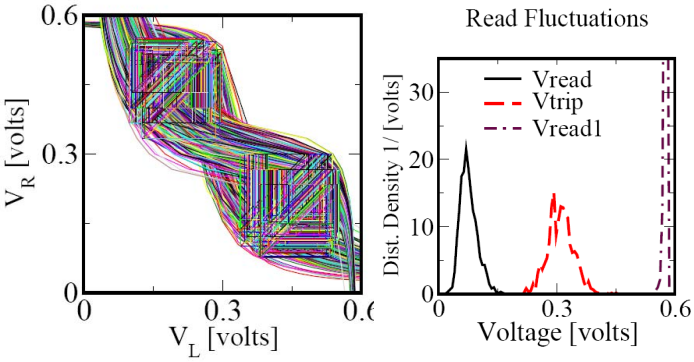

Fig 6a (above left): Static voltage characteristics of 512 A cells at 600mV during a Read operation *with SNM for each cell.*
Fig 6b (above right): Fluctuations of the three roots (defined in Fig 1b)

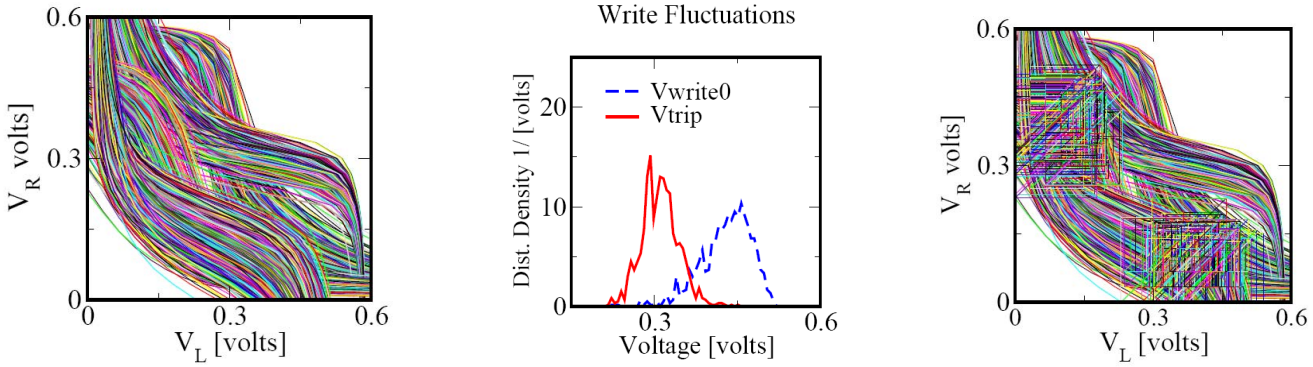

Fig 7a (above left): Static voltage characteristics of 512 A cells at 600mV during a Write operation **Fig 7b** (above center): Distributions of the Write0 (defined in Fig 3) and Trip voltage distributions **Fig 7c** (above right): Static voltage characteristics of 512 A cells at 600mV during a Write operation *with WNM for each cell.*

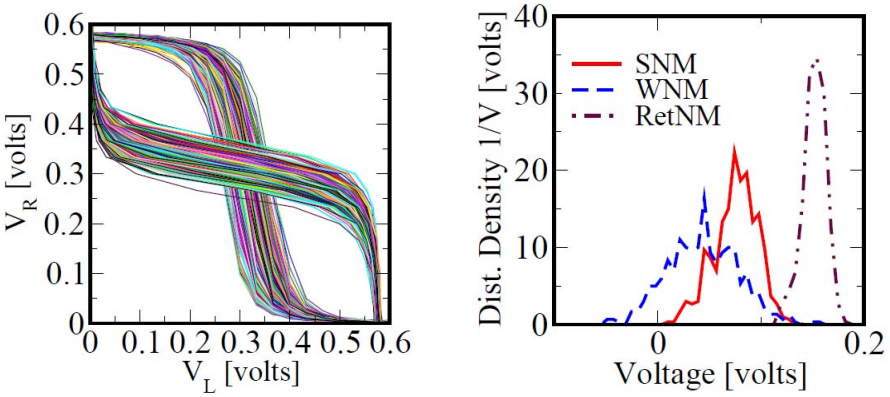

Fig 8a (above left): Static Voltage Characteristics of 512 A cells during Retention (WL=0).

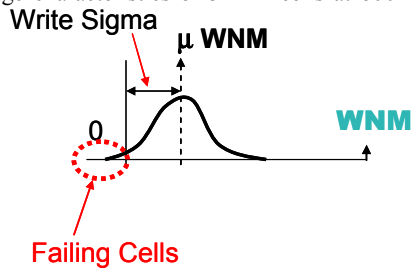

Fig 8b (at left): Measured WNM, SNM & Retention Noise Margin (RetNM) distributions. Distributions demonstrate A cells to be most limited by Write and least by Retention fluctuations. Fraction of distribution to the left of the origin (**Fig 9** above) corresponds to failing cells.

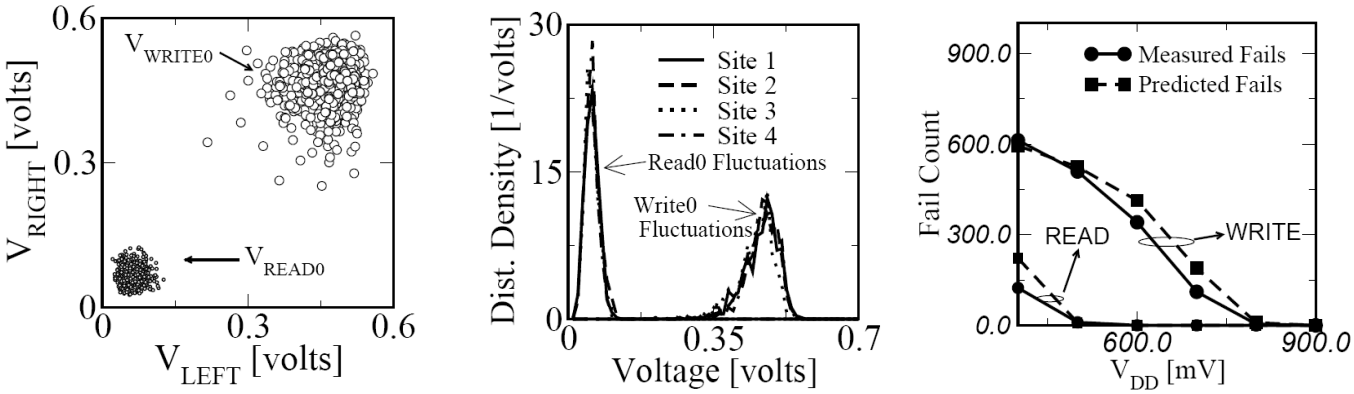

Fig 10 (above left): Left-Right correlation coeff. of 0.003 and 0.005 for Vread0 and Vwrite0 demonstrate the measured fluctuations to be overwhelmingly random**. Fig 11 (above center):** Fluctuation distributions of Read0 and Write0 measured from 4 different sites demonstrate fluctuations to be reproducible. **Fig 12 (above right):** The SNM and WNM distribution sigma and mean are applied to predict the R/W fail counts from a sample of 1024 B cells. These are compared with the actual R/W fail counts in the same sample.

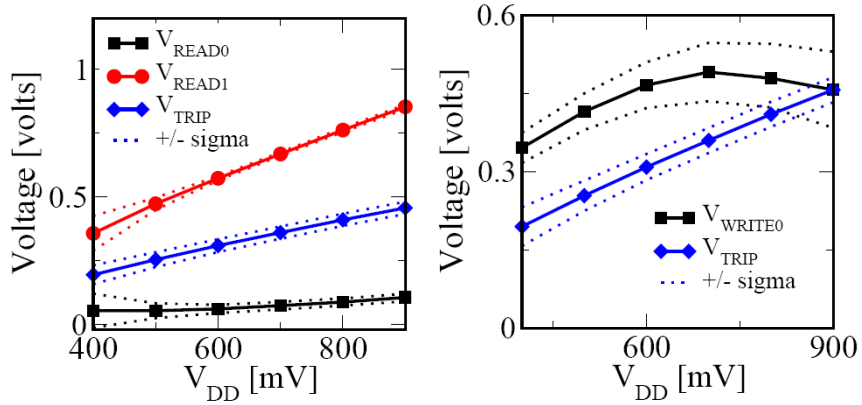

Fig 13-14: Measured Read (Far left) and Write (at left) fluctuation dependencies on operating voltage demonstrate rapid decline in DC margin and DC yield

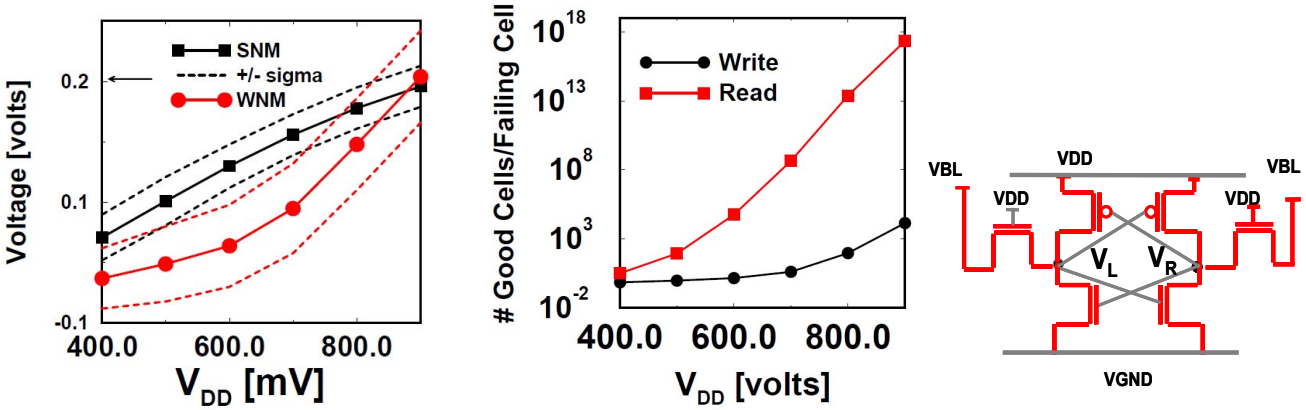

Fig 15-16(above left, center): Measured WNM and SNM decrease while their variance remains mostly unchanged with operating voltage resulting in a rapid decline of yield. **Fig 17** (above right) Cell biased to improve fluctuation immunity

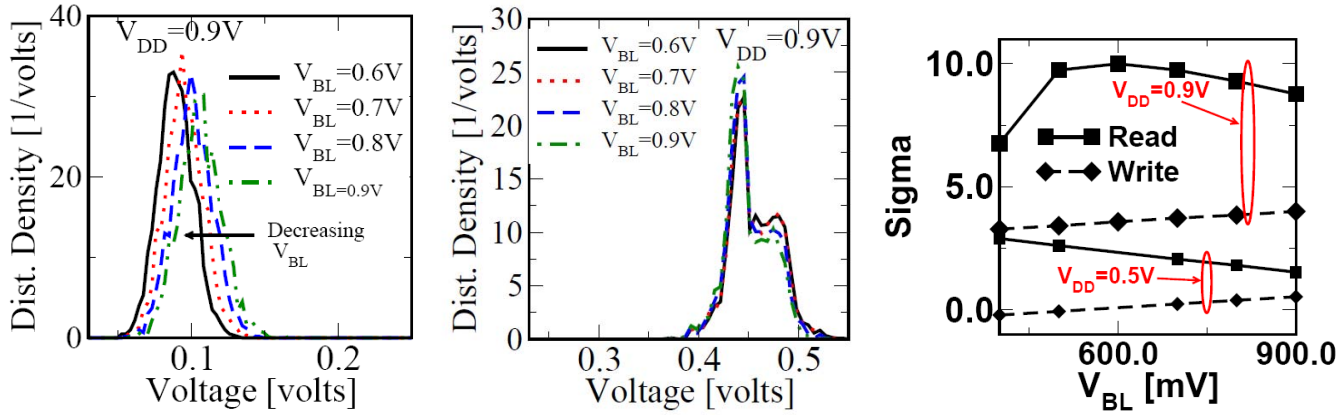

Fig 18 (above left): Read0 distributions move to the left at lower VBL reducing their overlap with Vtrip distributions **Fig 19** (above center): VTRIP distributions remain mostly unaffected by a lowered BL precharge. **Fig. 20**(above right): Optimal VBL during Read equals VDD-VT. Read Sigma=μSNM/σSNM. Circuit Schemes where the BL is driven to VDD by data-in during the Write window (WL=VDD) would not permit any degradation in Write Margin seen in Fig 20 above.

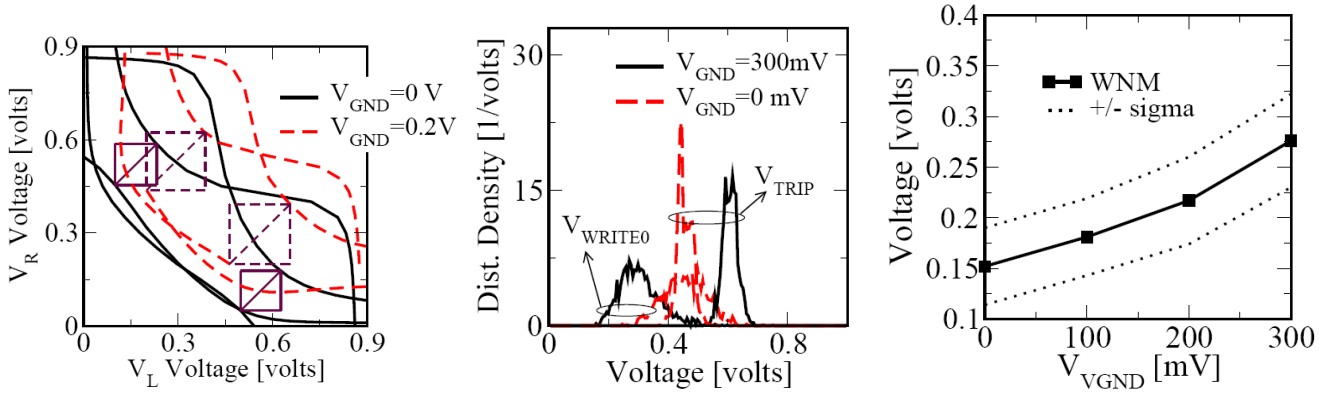

Fig 21 (above left) Write characteristics at 0.9V with conventional operation.(solid) and with '***Write Assist'*** - raised VGND only during Write operations and during Retention (dashed) **Fig 22-23** (above center, right) '***Write Assist***' raises VTRIP and lowers VWrite0 improving write margins

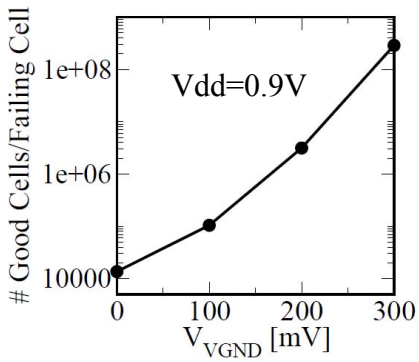

Fig 24 (at left) : '***Write Assist'*** lowers Write Fail Count by over 4 orders of magnitude. With a raised VGND, unaccessed cells that share the same column (using a common VGND rail) see a lower rail-rail voltage. VGND may be raised until the decreasing Retention sigma with VDD-VGND across the unaccessed cells (Fig 8) equals the increasing Write sigma.